

Laptop Schematics

www.Telegram.me/schematics_laptop

Compal Confidential

SLC M/B Schematics Document

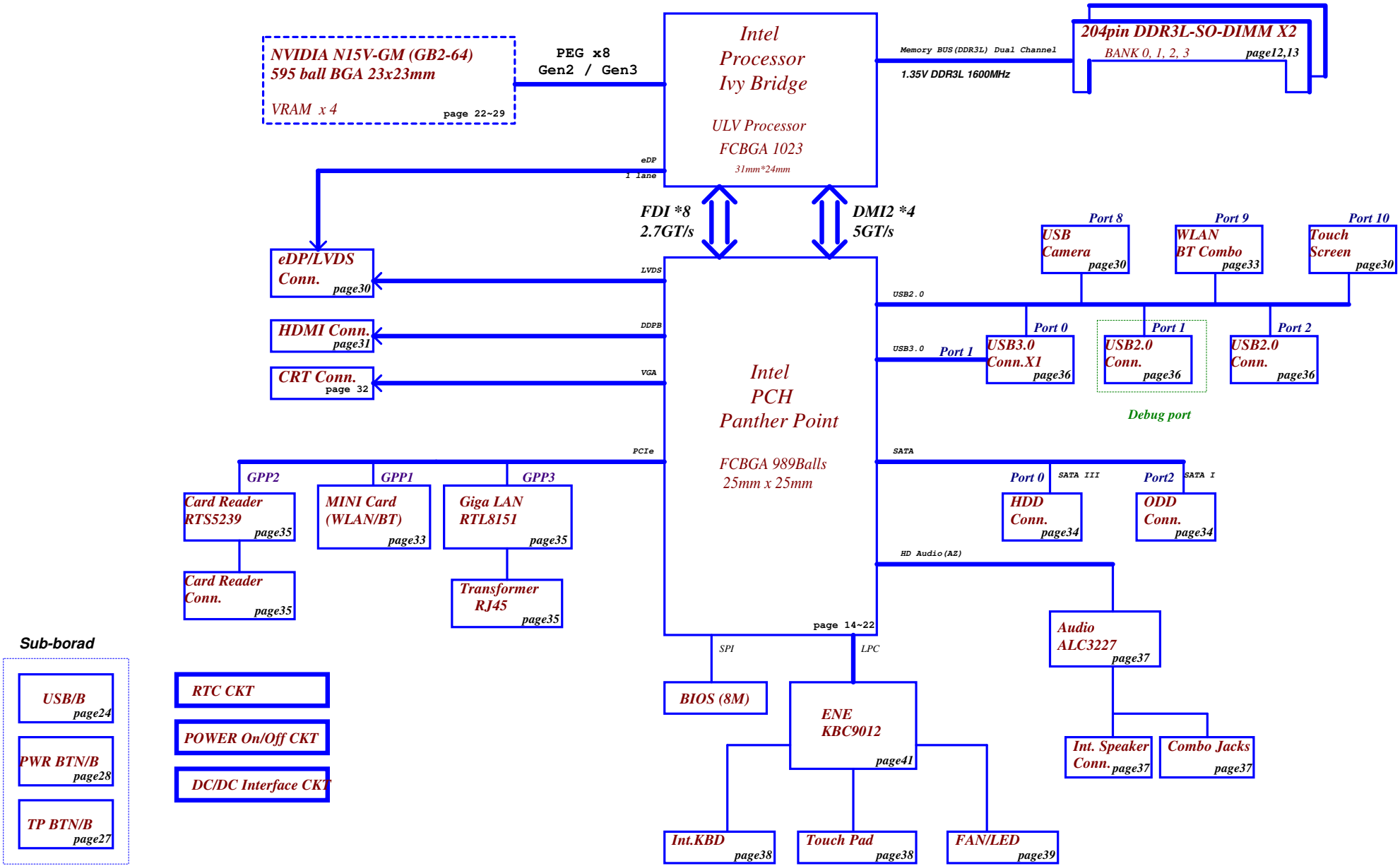
14": Tabo; 15.6" Pochacco

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2013/11/13

Version 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Block Diagrams
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-A999P	Rev 0.1
				Date Friday, March 14, 2014	Sheet 1 of 58



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title	Block Diagrams	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-A999P	0.1
				Date:	Friday, March 14, 2014	Sheet 2 of 58

ZSO40/50 (LA-A998P/LA-A999 Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.675VS	+0.675VP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.35V	+1.35V_VDDQP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+3VALW) to 1.8V LDO power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VL to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+3VGS	GPU power	PX	OFF	OFF
+VGA_CORE	GPU power	PX	OFF	OFF
+1.05VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52
Charger IC BQ24738	0xFFH

EC SM Bus2 address

Device	Address
PCH SML1	
N15V-GE dGPU	

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	

SMBUS Control Table

	SOURCE	BATT	WLAN MIIN1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	dGPU	
EC_SMB_CK1 EC_SMB_DA1	KB9012	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB9012							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH					V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	mini WLAN	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE2	PCIE LAN	CLKOUTFLEX3	DGPU_PRSNT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :
: means Digital Ground
: means Analog Ground

Project ID	UMA@	DIS@		
------------	------	------	--	--

PCB	LA-A998P	LA-A999P
	14@	15@

BY SKU		
TPM	9635@	9656@
CPU	CPUUMA1@ CPUUMA2@ CPUDIS@	
VRAM	X76@ MIC@	SAM@ HY@

Option	@	CONN@	SP@	PX@	UMA@	DIS@	
UMA	X	X	V	X	V	X	
DIS	X	X	V	V	X	V	

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC/TPM
PCI2	None
PCI3	None
PCI4	None

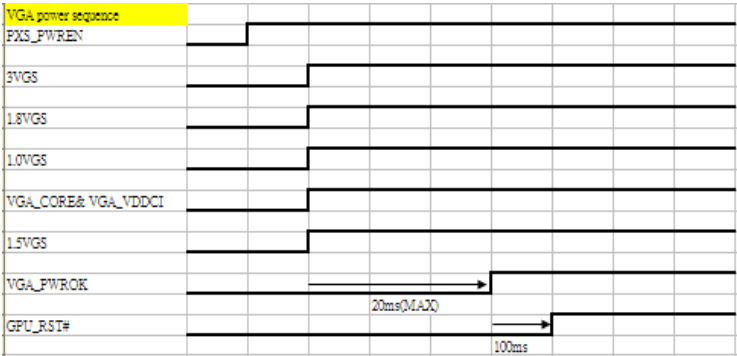
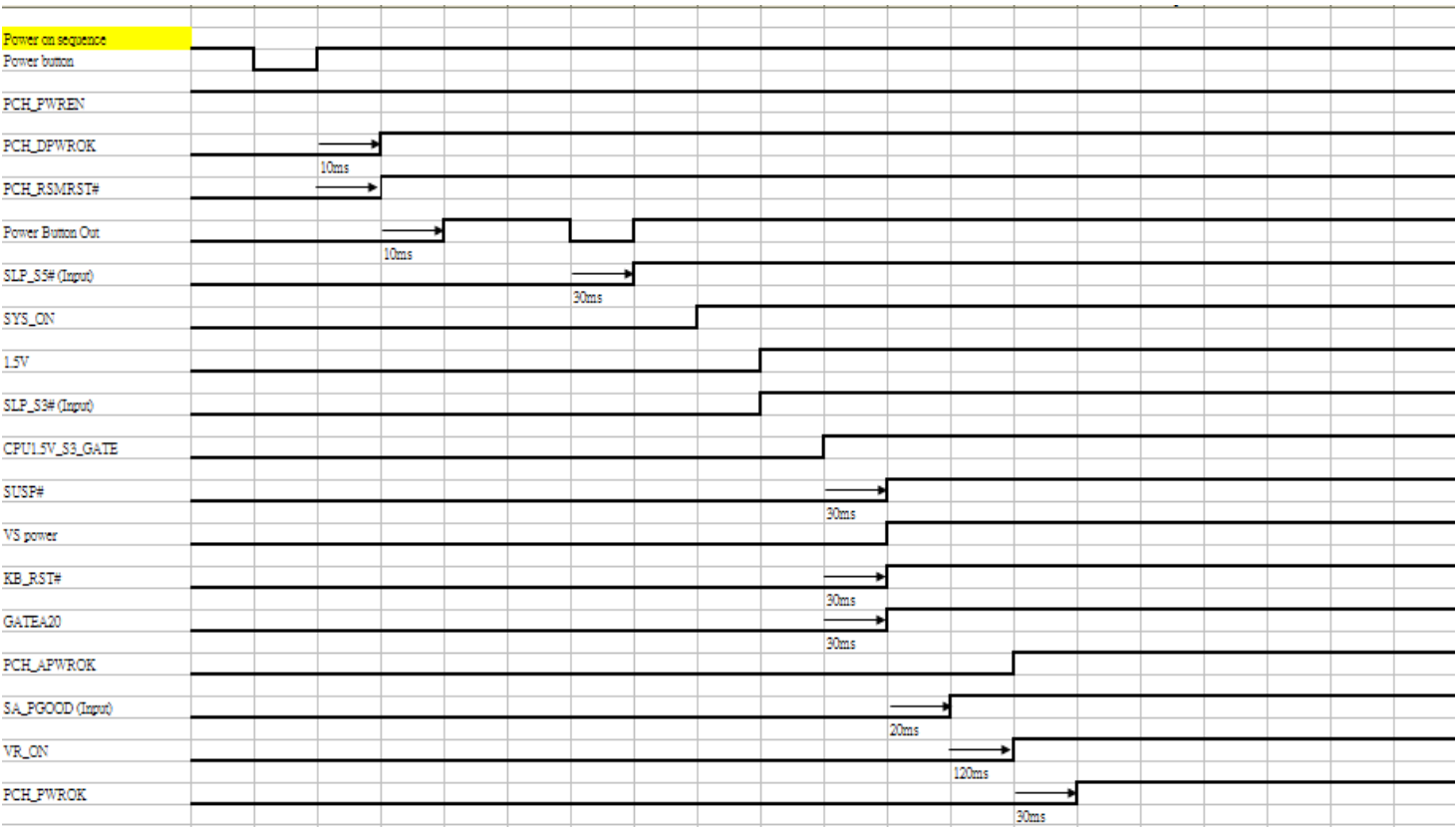
SATA	DESTINATION
SATA0	JHDD1
SATA1	None
SATA2	JODD1
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (For USB3.0 Conn.)
		1	USB2.0 (D/B)
	UHCI1	2	USB2.0 (D/B)
		3	None
	UHCI2	4	None
		5	None
EHCI2	UHCI3	6	None
		7	None
	UHCI4	8	Camera
		9	Mini Card(WLAN& BT)
	UHCI5	10	Touch Screen
		11	None
	UHCI6	12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	None
	4	None

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2011/06/29	Deciphered Date	2011/06/29		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Notes List		
					Size	Document Number	Rev
					LA-A999P		0.1
Date:		Friday, March 14, 2014		Sheet	3	of 58	



Security Classification		Compal Secret Data			
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	PROCESSOR(1/7) DMI,FDI,PEG
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Rev	0.1
Date: Friday, March 14, 2014		Sheet 4 of 58			

UCPU1 CPUDIS01@
i5-2467M CPU
SA00004X000

UCPU1 CPUDIS02@
i5-2367M CPU
SA000051H20

UCPU1 CPUDIS03@
i5-2367M CPU
SA000051H20

UCPU1 CPUDIS04@
i5-3317U CPU
SA00005K600

UCPU1 CPUUMA3@
i5-2367M CPU
SA000051H20

UCPU1 CPUUMA1@
17W 1.5GHz GT2 ES2 QBP8
SA00005AZ10

UCPU1 CPUUMA4@
17W 1.7GHz no onfig ES2 QBP7
SA00005B010

UCPU1 CPUUMA2@
17W 1.5GHz no onfig ES2 QBTB
SA00005AZ20

UCPU1 CPUUMA5@
17W 1.7GHz no onfig ES2 QBTQ
SA00005B020

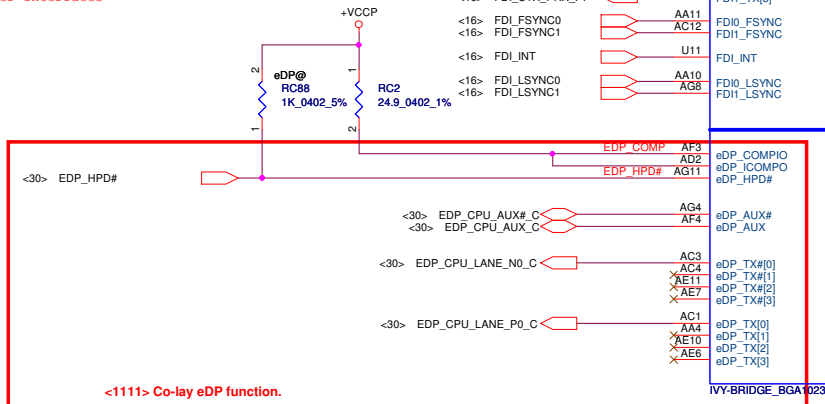
Sandy Bridge:
Intel Core i5-2467M: SA00004X000 (4619HY32L01)

Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QBTB: SA00005AZ20(4619HZ32L02)

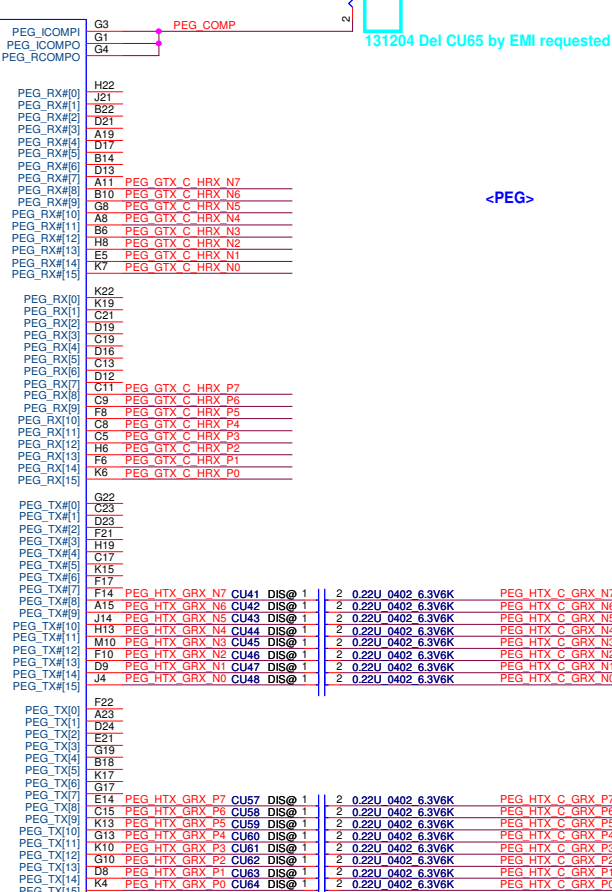
PEG_ICOMPI and RCOMPO signals should be
shorted and routed
with - max length = 500 mils - typical
impedance = 43 mohms
PEG_ICOMPO signals should be routed with -
max length = 500 mils
- typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals
should be shorted near balls
and routed with typical
impedance <25 mohms

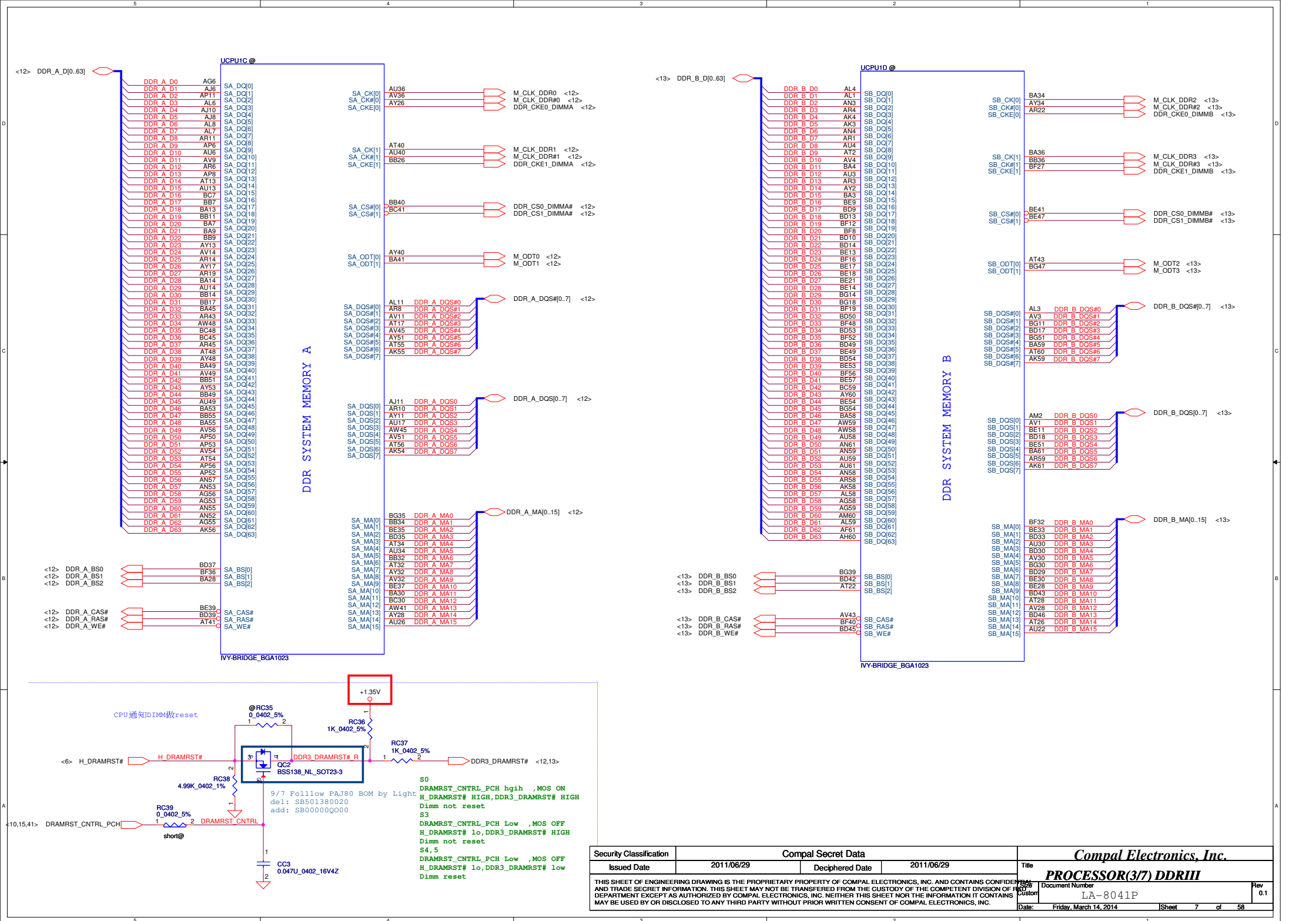
NOTE:eDP_COMPIO and eDP_ICOMPO
should not be left floating even if Internal
Graphic is disabled since they are shared
with other interfaces

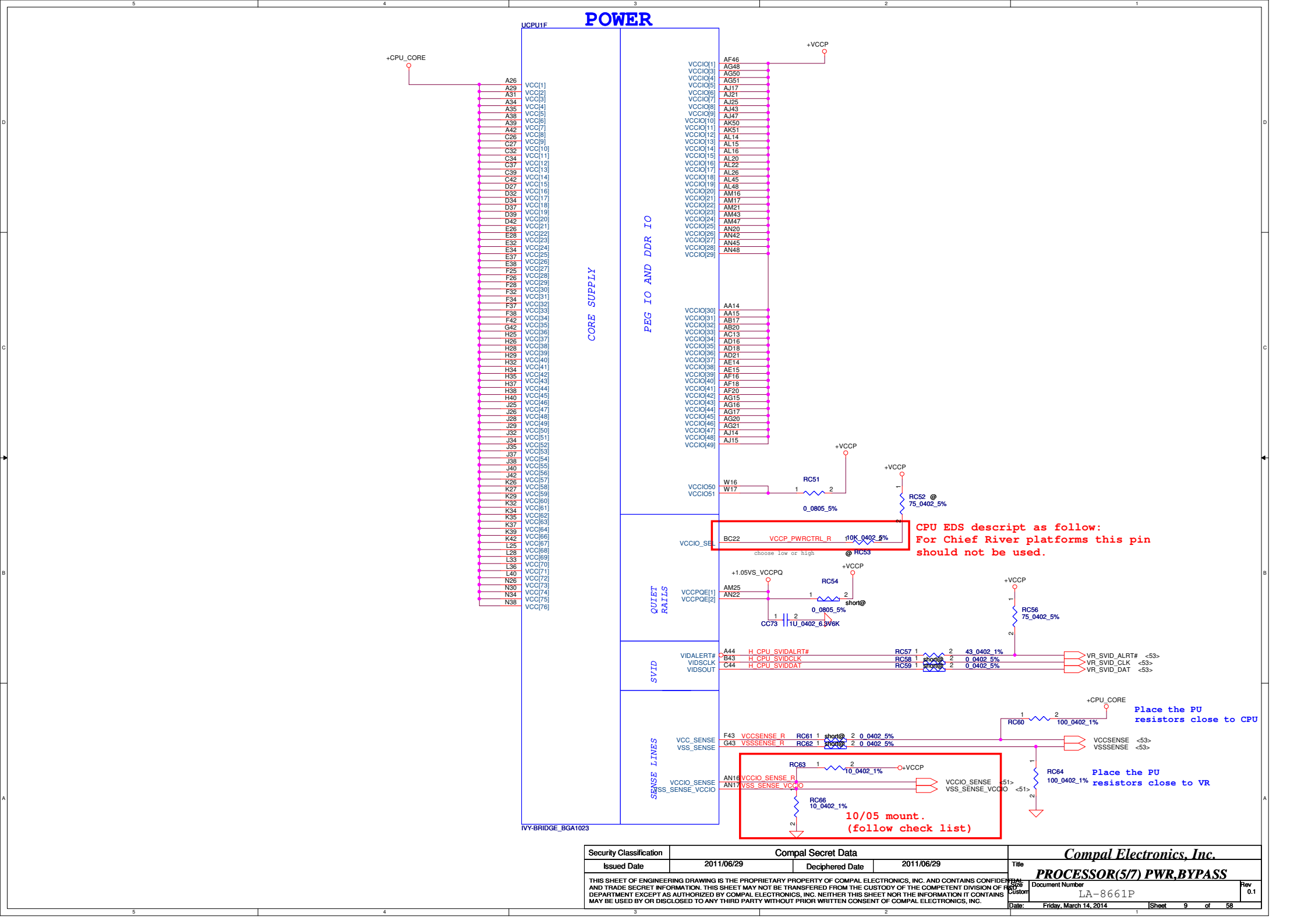


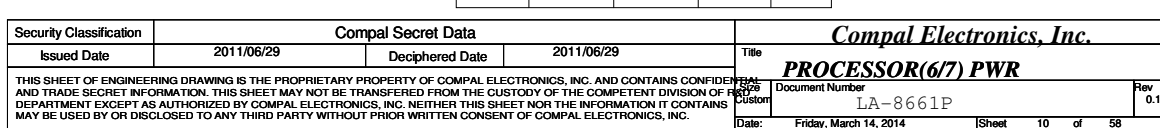
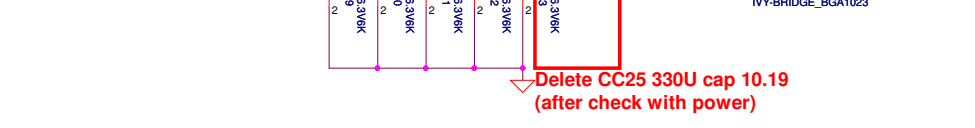
PCI EXPRESS -- GRAPHICS

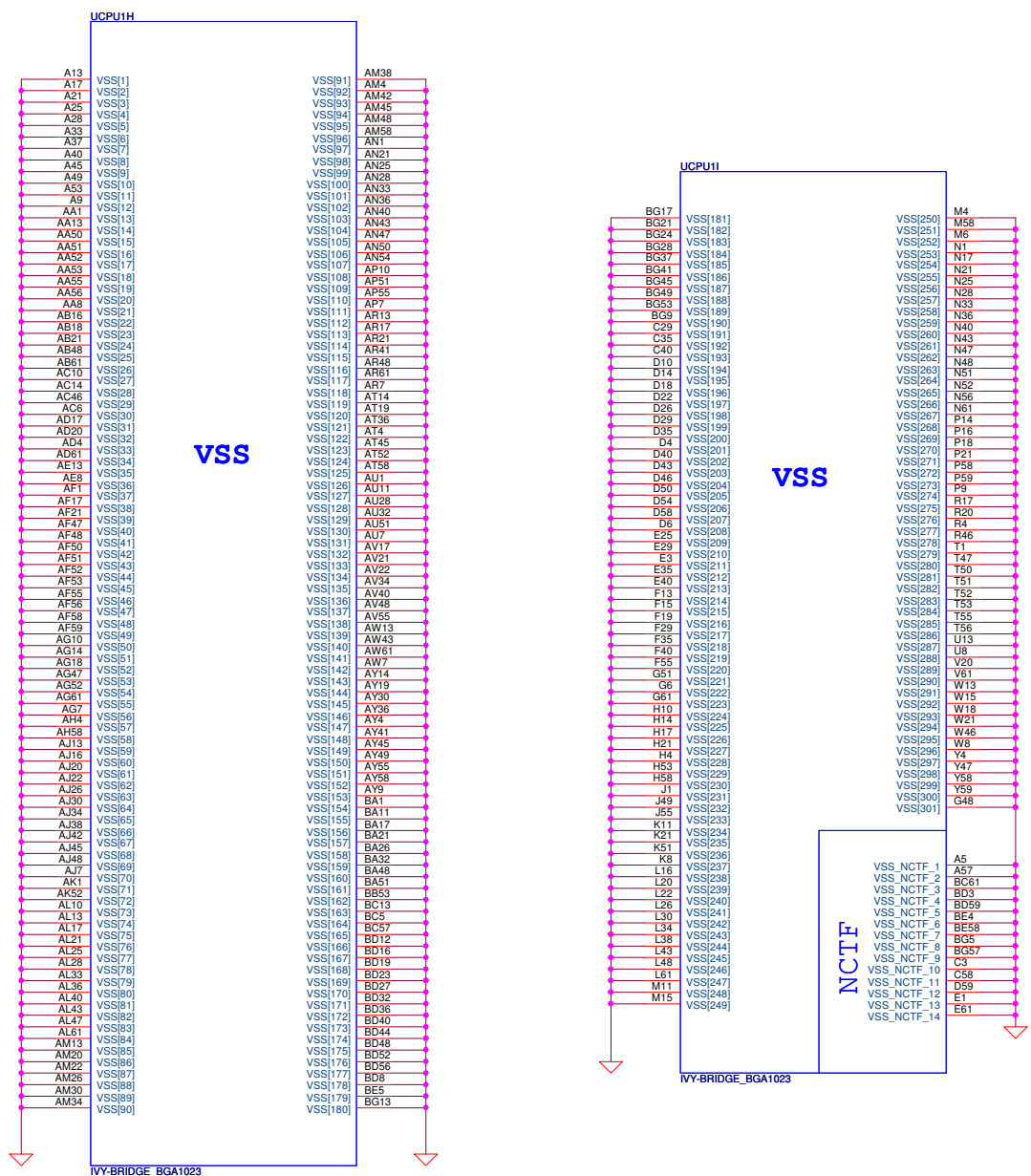


Typ- suggest 220nF. The change in AC capacitor
value from 180nF to 265nF is to enable
compatibility with future platforms having PCIe
Gen3 (8GT/s)

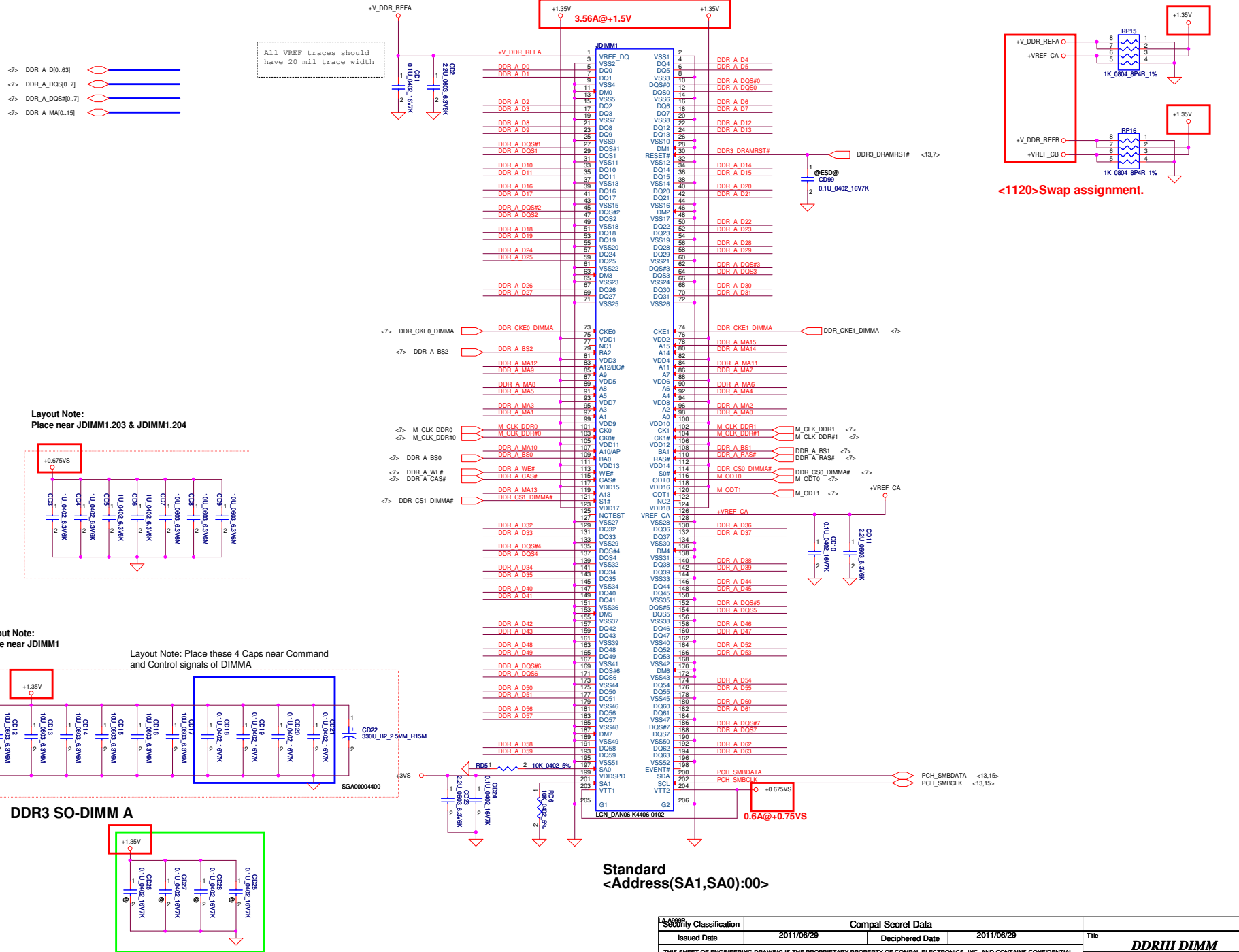




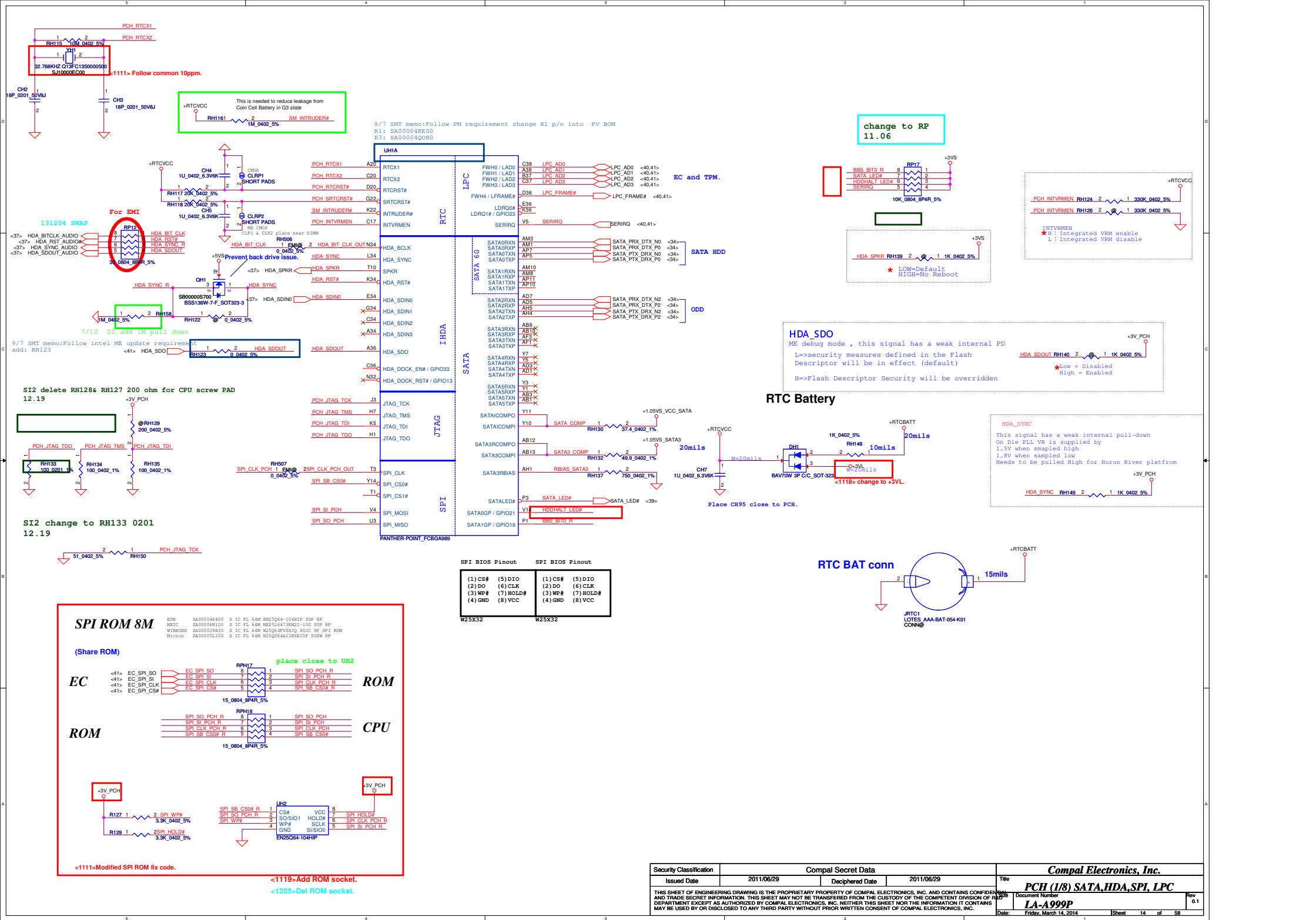


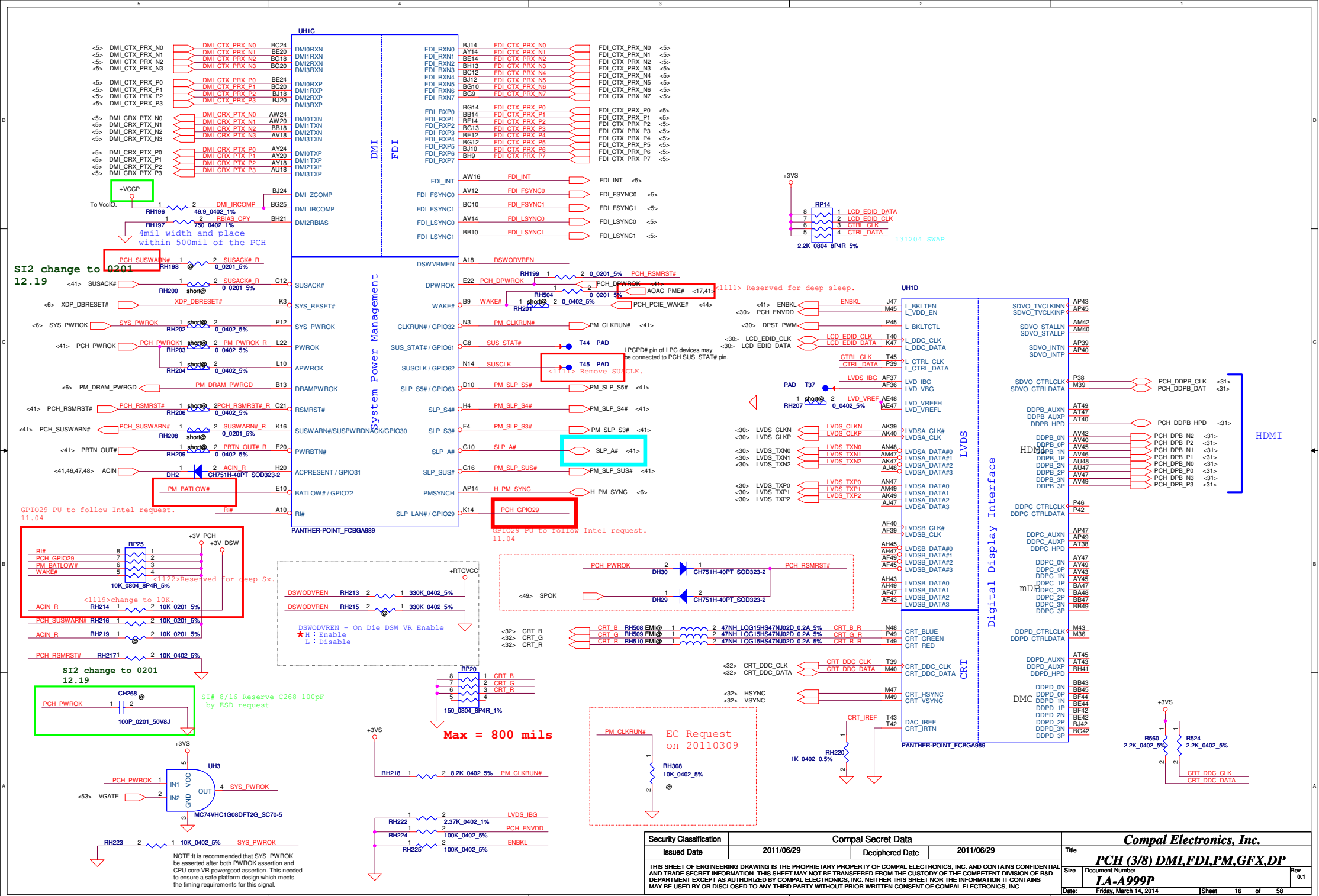


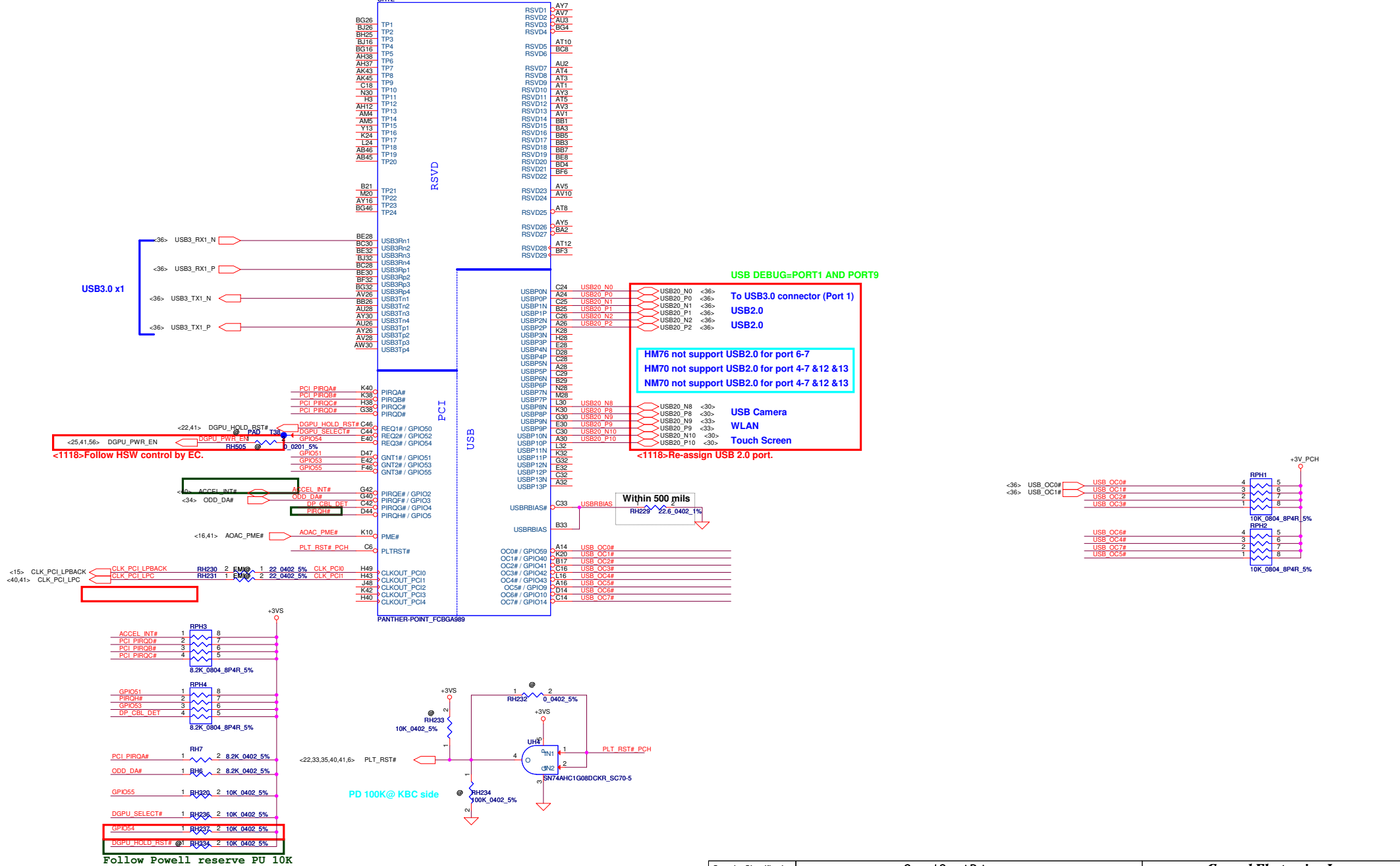
DDR3 SO-DIMM A



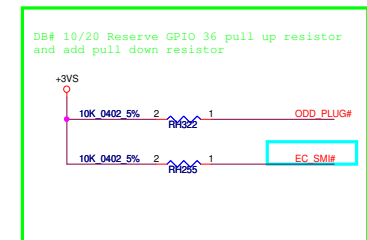
<div>LA-00999</div> <div>Security Classification</div>		<div>Compul Secret Data</div>		<div>Title</div>	
<div>Issued Date</div>		<div>Deciphered Date</div>		<div>2011/06/29</div>	
<div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPLETE DIVISION OF R&D TO ANY OTHER DIVISION OR AUTHORIZED BY COMPAL ELECTRONICS, INC. NOR THE INFORMATION CONTAINED HEREIN MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div>				<div> <div>Size</div> <div>Document Number</div> <div>LA-8661P</div> <div> <div>Rev</div> <div>0.1</div> </div> </div>	
<div>P-0000</div>		<div>Expiry Month</div>		<div>12/0000</div>	





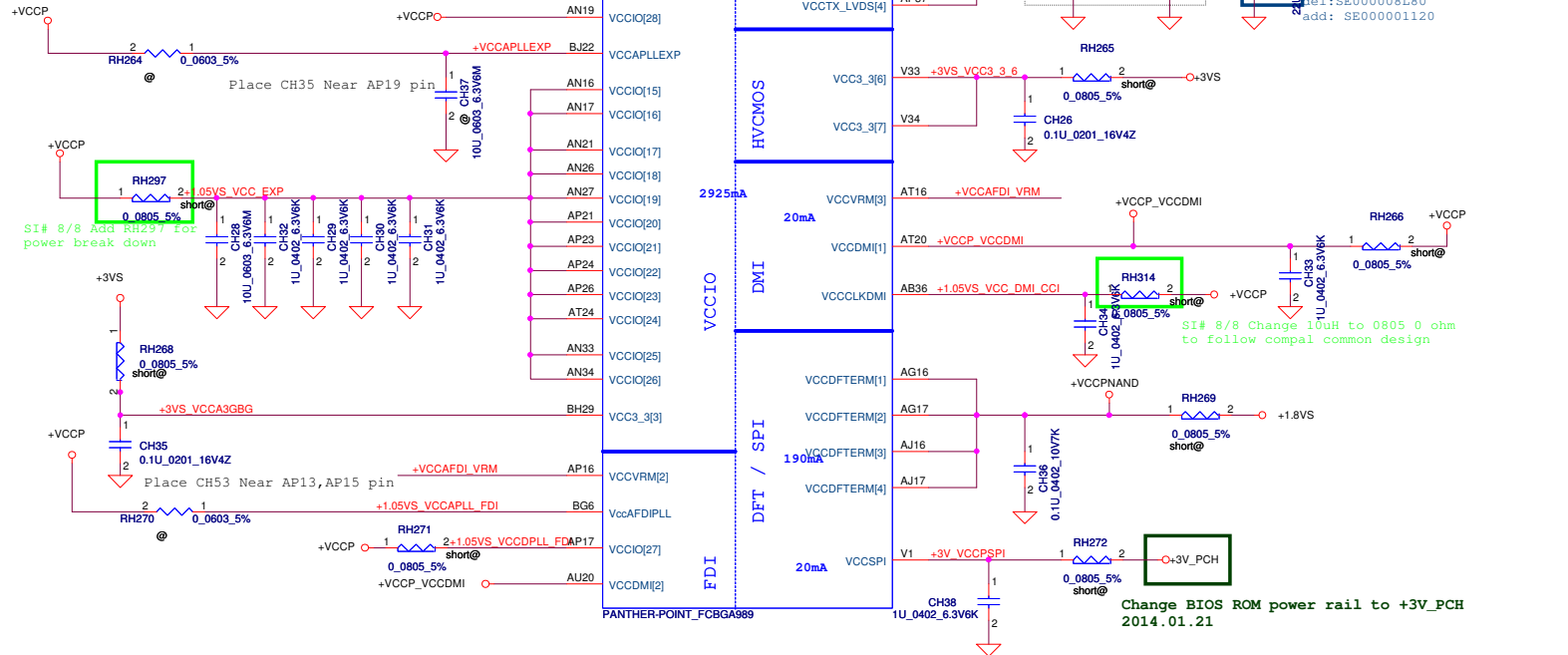


Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Size	
2011/06/29		2011/06/29		Document Number	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Compal Electronics, Inc.		Rev	
		PCH (4/8) PCI, USB, NVRAM		0.1	
		LA-A999P		Date	
		Friday, March 14, 2014		Sheet 17 of 58	

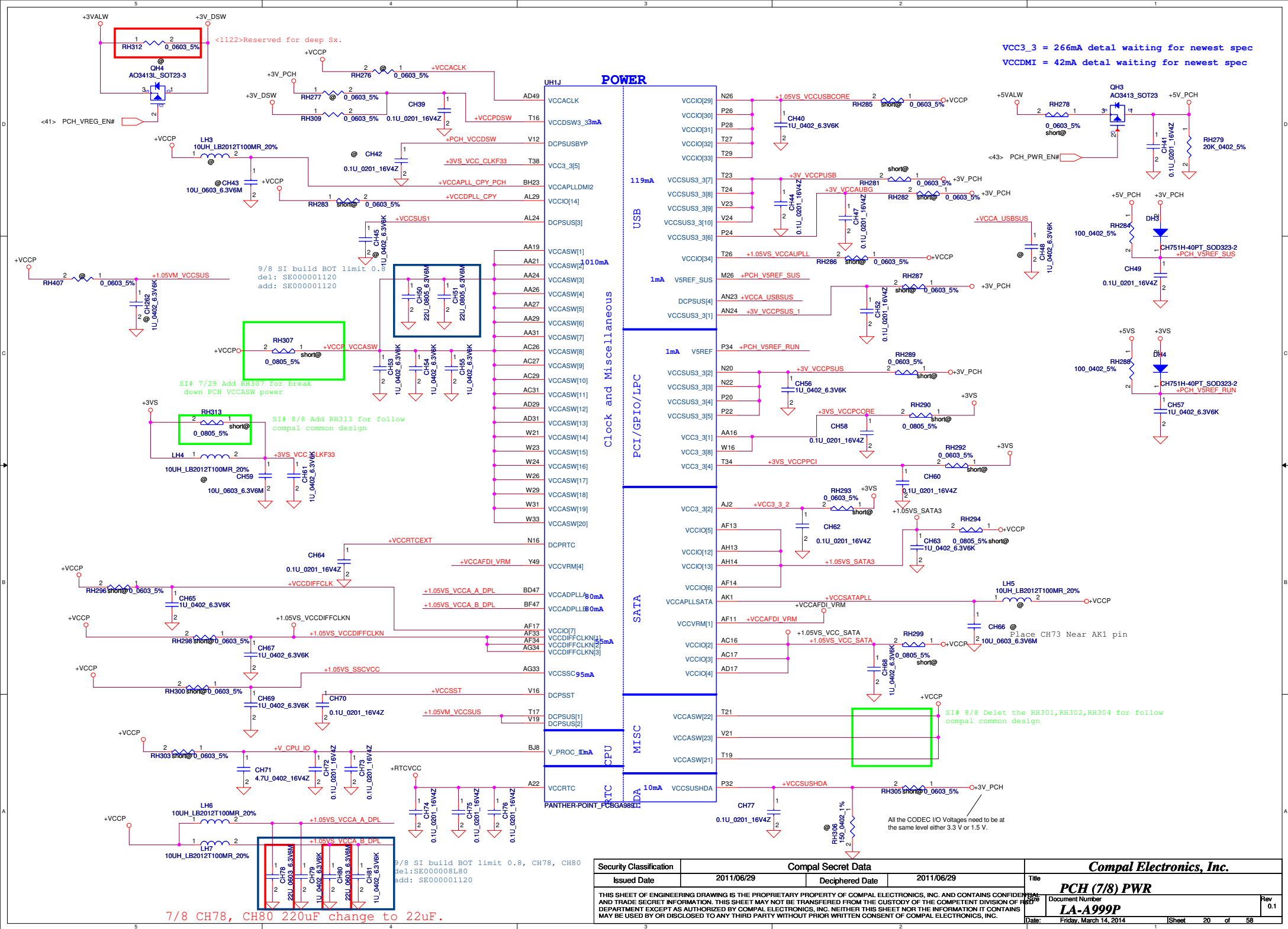


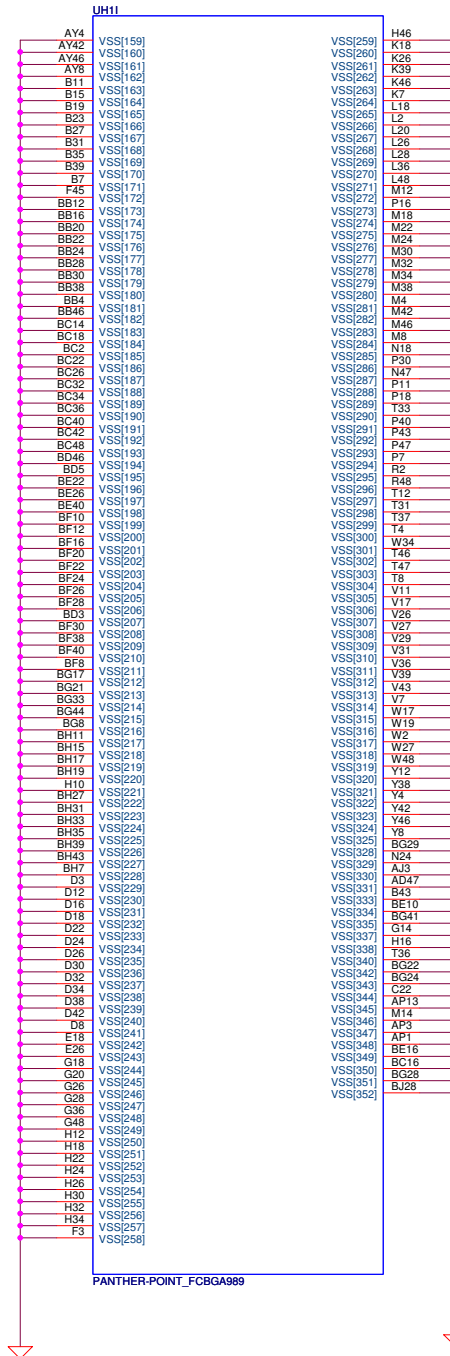
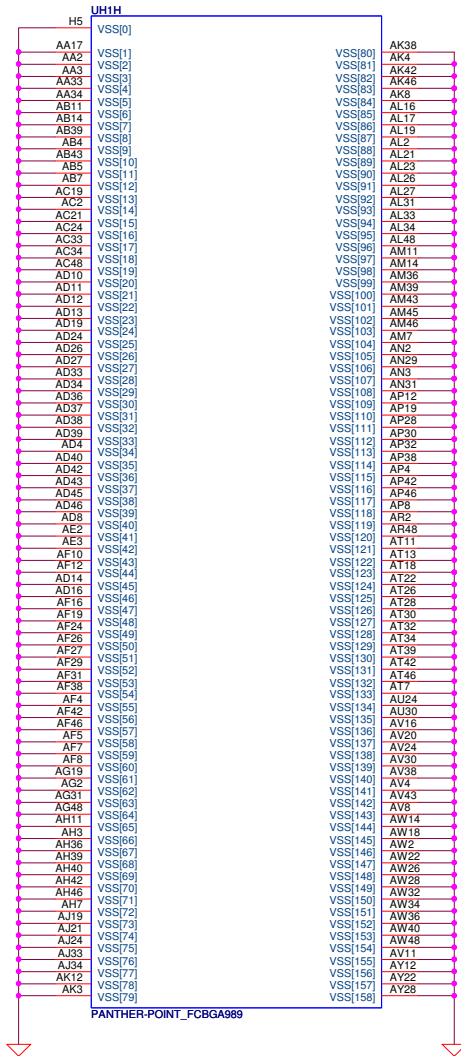
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	PCH (5/8) GPIO, CPU, MISC	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					LA-A999P	0.1
				Date:	Friday, March 14, 2014	Sheet 18 of 58

2011.10.18 change all cap to small size:
22u& 10u to 0603
4.7u to 0402
1u, 0.1u, 0.01u to 0201



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	PCH (8/8) VSS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-A999P
				Rev	0.1
				Date:	Friday, March 14, 2014
				Sheet	21 of 58

<CPU>

<CPU>

<CPU>

Differential signal

Controlled by EC "AND" PCH

SI 11/05 change RV182.1
change to +3VGS from GPU_PWR_EN

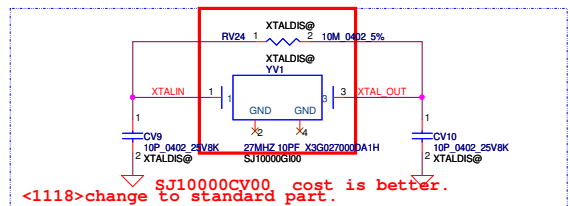
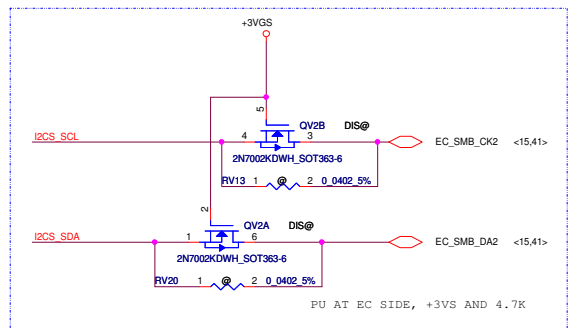
#9/2 , Add RV191 between.
GPU_PWR_LEVEL# and GPU_THERMAL_DET#

#8/19 ,N15V-GM didn't support GC6,
unpop QV13 ,QV14.

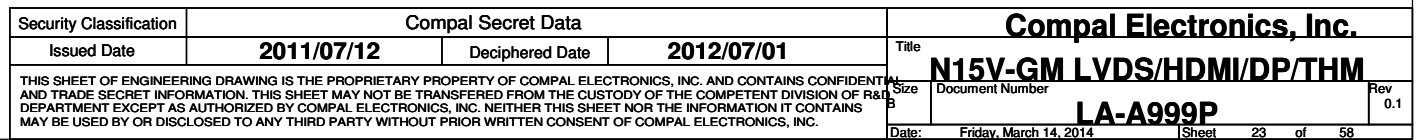
131127 SWAP Pin of RV36.1, RV36.2 & RV36.4 by layout requested

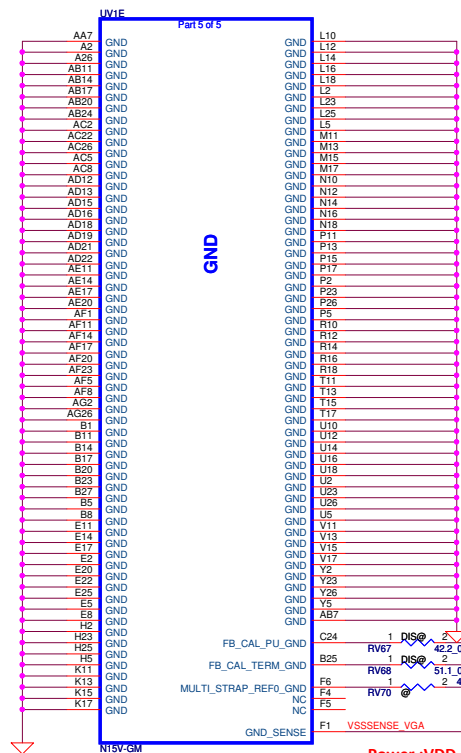
#08/22,unused I2C change to pull-down.

#08/22,unused I2C change to pull-down.



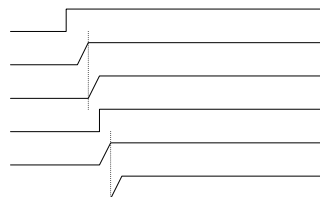
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	0.1
				Date	Friday, March 14, 2014
				Sheet	22 of 58





Power on

DGPU_PWR_EN
+3VGS
+VGA_CORE
DGPU_PWROK
+1.05VGS
+1.5VGS



40us < Rt < 2ms

<18,56> DGPU_PWROK

#08/20 Don't support GC6, Add RV66. Unpop QV16, RV41, RV42, CV78.

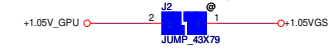
#8/19.RV70 unpop, N15V-GM use binary mode.

Contrl by power

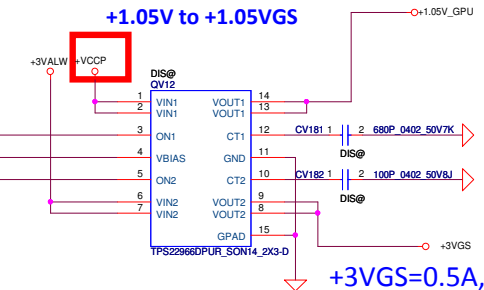
Power :VDD_SENSE & GND_SENSE
Differential signal

#8/20 : N15V-GM don't support GC6 function. UV20 unpop.

+1.05VGS=1.6A,4vias.

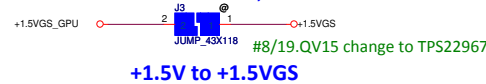


+3VALW to +3VGS
+1.05V to +1.05VGS



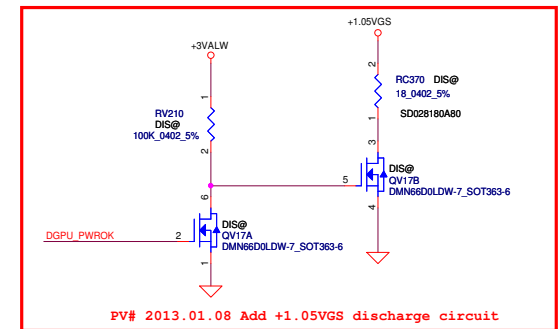
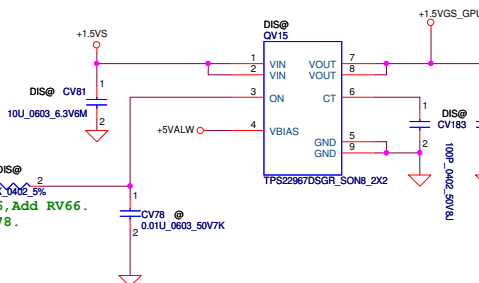
+3VGS=0.5A,2vias.

+1.5VGS=3.6A,8vias.



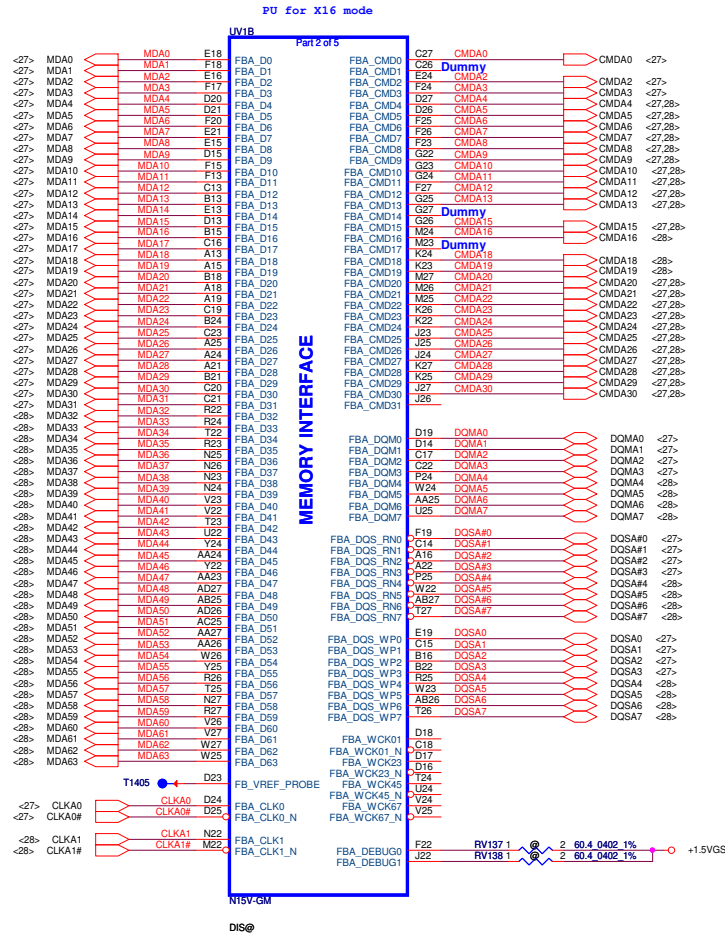
#8/19.QV15 change to TPS22967

+1.5V to +1.5VGS



PV# 2013.01.08 Add +1.05VGS discharge circuit

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N15V-GM VGA CORE, GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Rev	0.1
				Date	Friday, March 14, 2014
				Sheet	25 of 58



Mode D Command Mapping

RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18	ODT	
FBx_CMD19	CKE	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

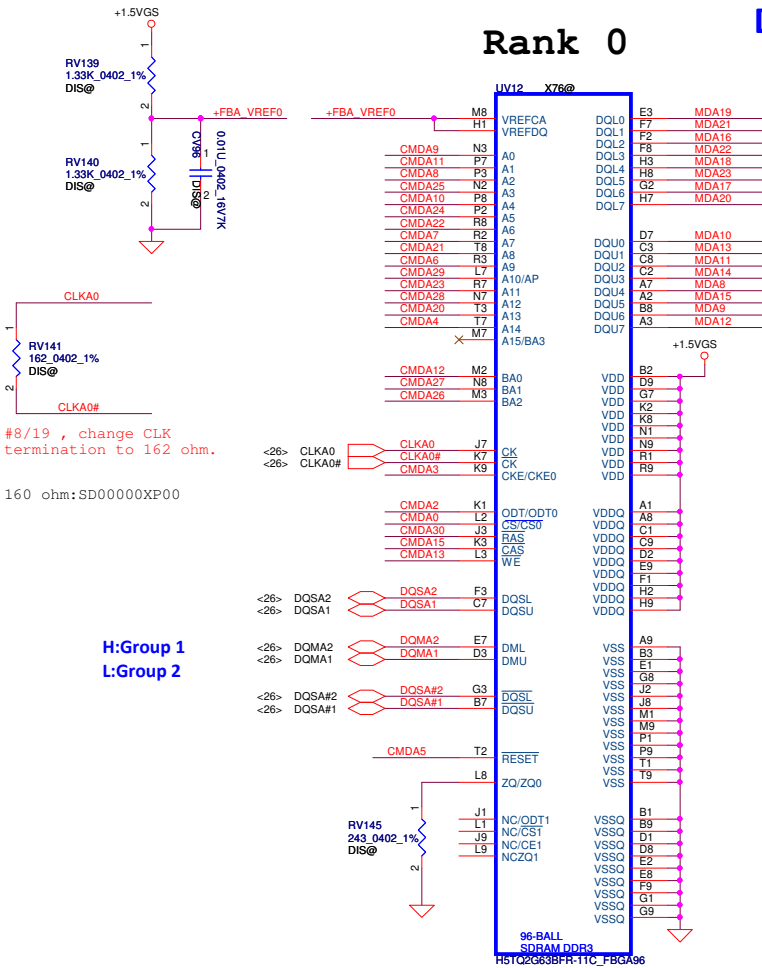
Memory Partition A RANK 0

Data0~Data31

MDA[0..63] <26,28>
CMDA[30..0] <26,28>

Rank 0

Rank 0

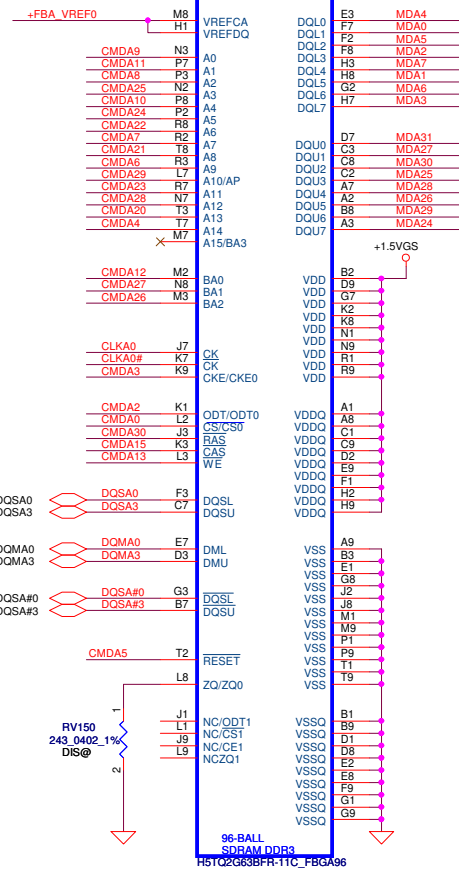


Group 2

Group 1

H:Group 1
L:Group 2

L:Group 0
H:Group 3



Group 0

Group 3

Mode D Command Mapping

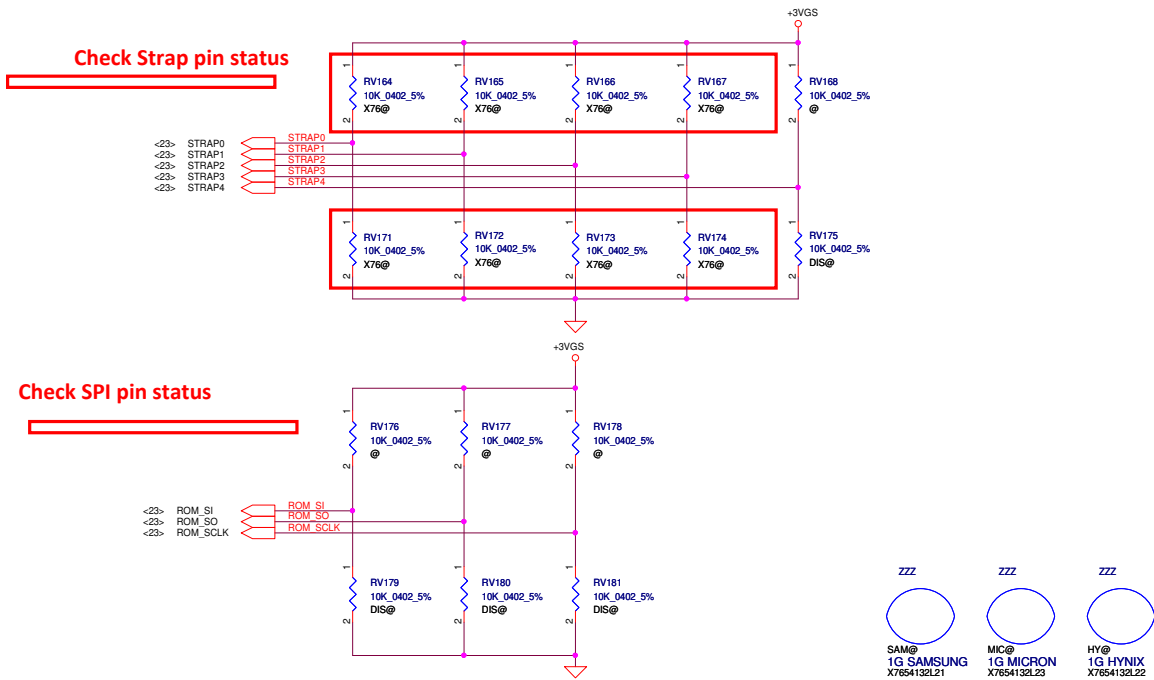
RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N15V-GM VRAM A Lower
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-A999P
				Date	Friday, March 14, 2014
				Sheet	27 of 58

Rank 0

Rank 0

	RANK 0	
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM CFG setup [3...0]	RAM_CFG	R P/N
N15V-GM (23x23) 64bit (One CH single rank)	ZSO40	128M(X16)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00006H400	H5TC2G63FFR-11C 1000MHz	1100	RV171+RV172+RV167+RV166	
	ZSO50	128M(X16)	CHA	DDR3 Micron 128Mx16 1.5V	SA000067500	MT41J128M16JT-093G-K 1000MHz	0001	RV164+RV172+RV173+RV174	
		128M(X16)	CHA	DDR3 Samsung 128Mx16 1.5V	SA000068U00	K4W2G1646E-BC1A 1000MHz	0101	RV164+RV172+RV166+RV174	

#9/5 RAM_CFG follow RVL-06891-001 table 1.
Dule Rank layout with single Rank population.

Table 123

Strap pin Name	Strap Mapping	Resistance	Polarity	Logical Strapping Bit0
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND.	
ROM_SI	SUB_VENDOR	10K	Pull-down to GND if no VBIOS ROM.	
ROM_SO	VGA_DEVICE	10K	Pull-down to GND(no diaplay).	
STRAP0	RAM_CFG[0]	10K		
STRAP1	RAM_CFG[1]	10K		
STRAP2	RAM_CFG[2]	10K		
STRAP3	RAM_CFG[3]	10K		
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND(PCIE Gen1).	

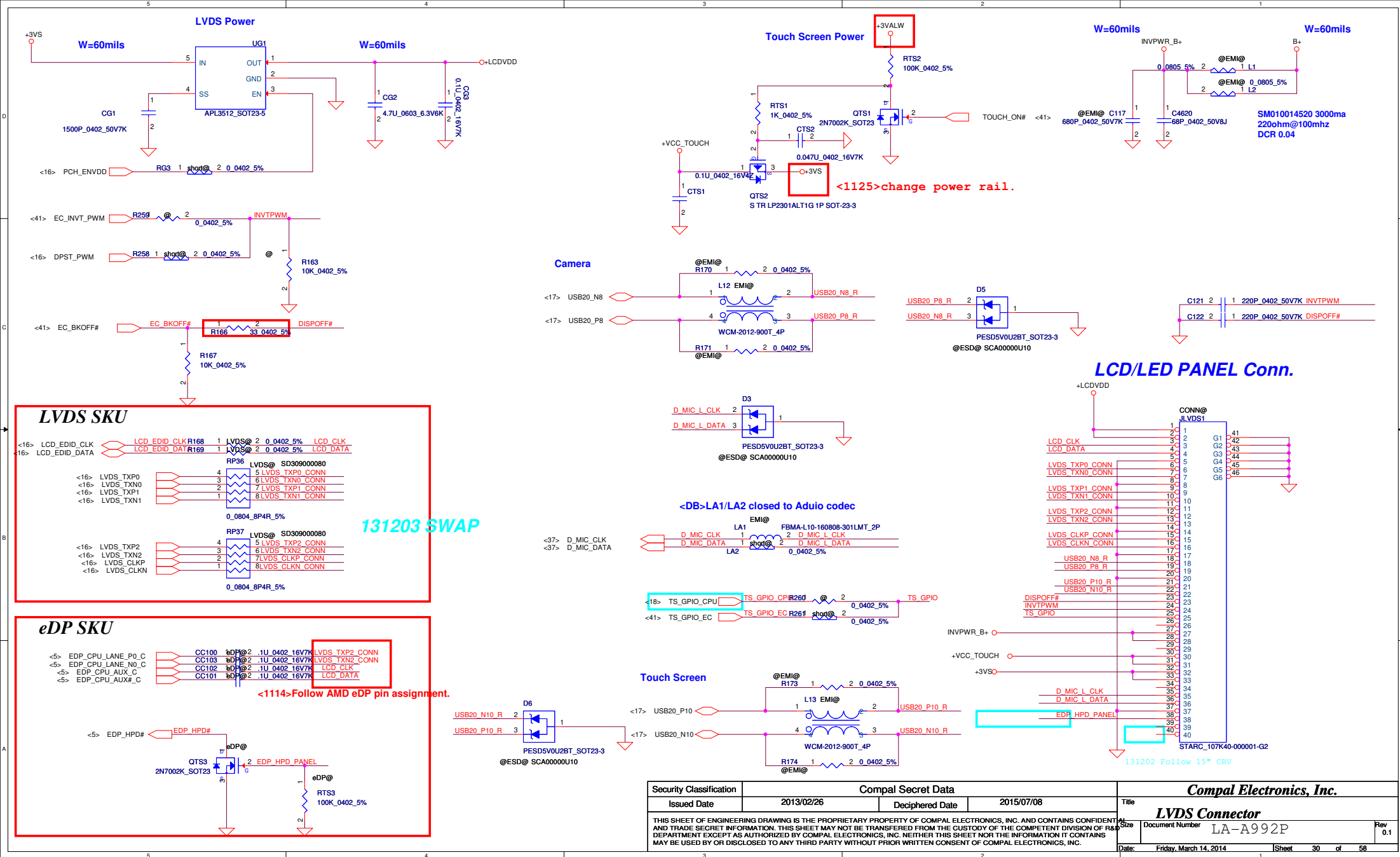
SMBUS_ALT_ADDR		SUB_VENDOR	
0	0x9E (Default)	0	Disable (Default)
1	0x9C (Multi-GPU usage)	1	

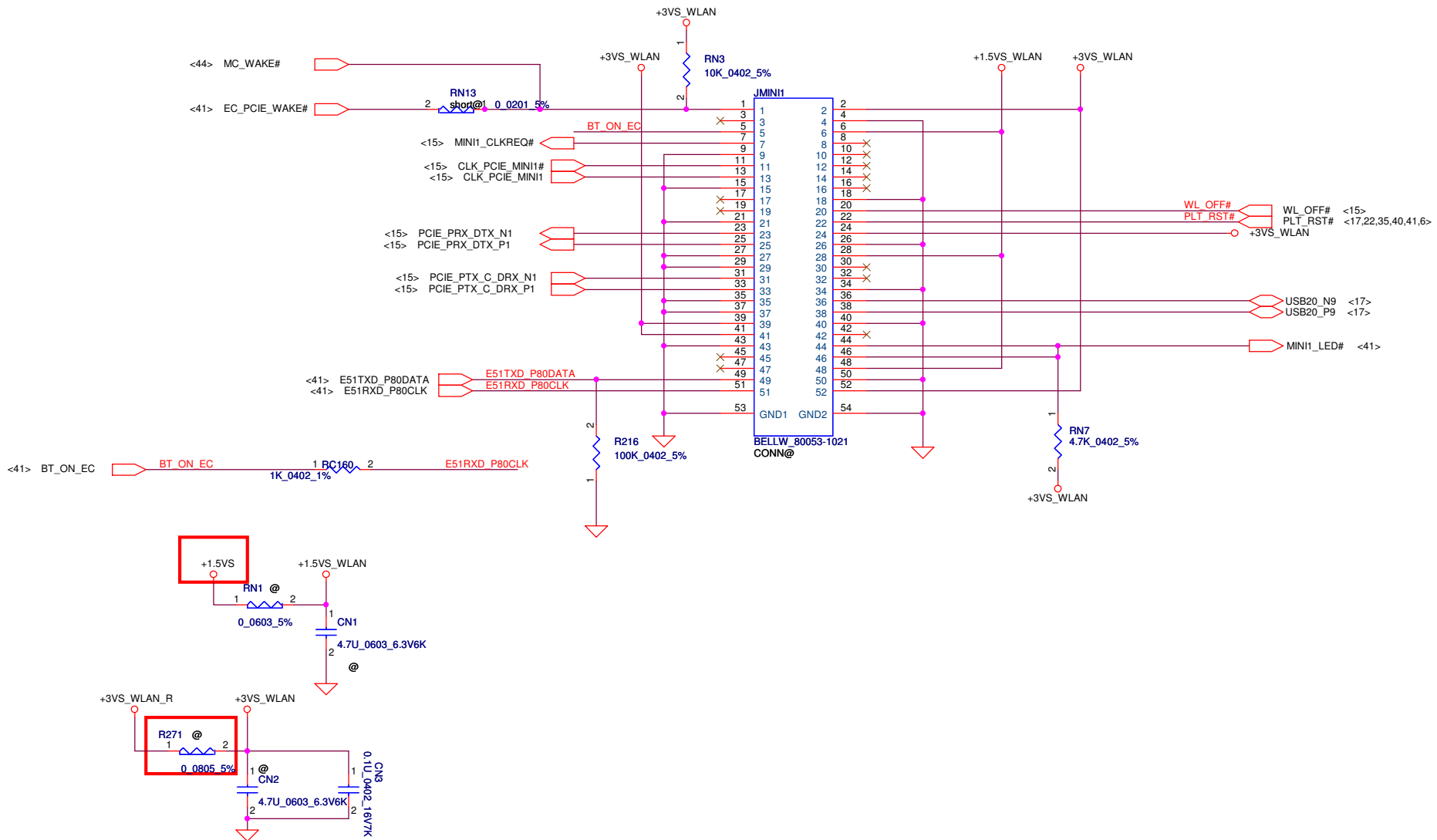
VGA_DEVICE	
0	Non-Primary 3D Acceleration Device(Class Code 302h)(Default)
1	Primary Display or VGA Device .

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

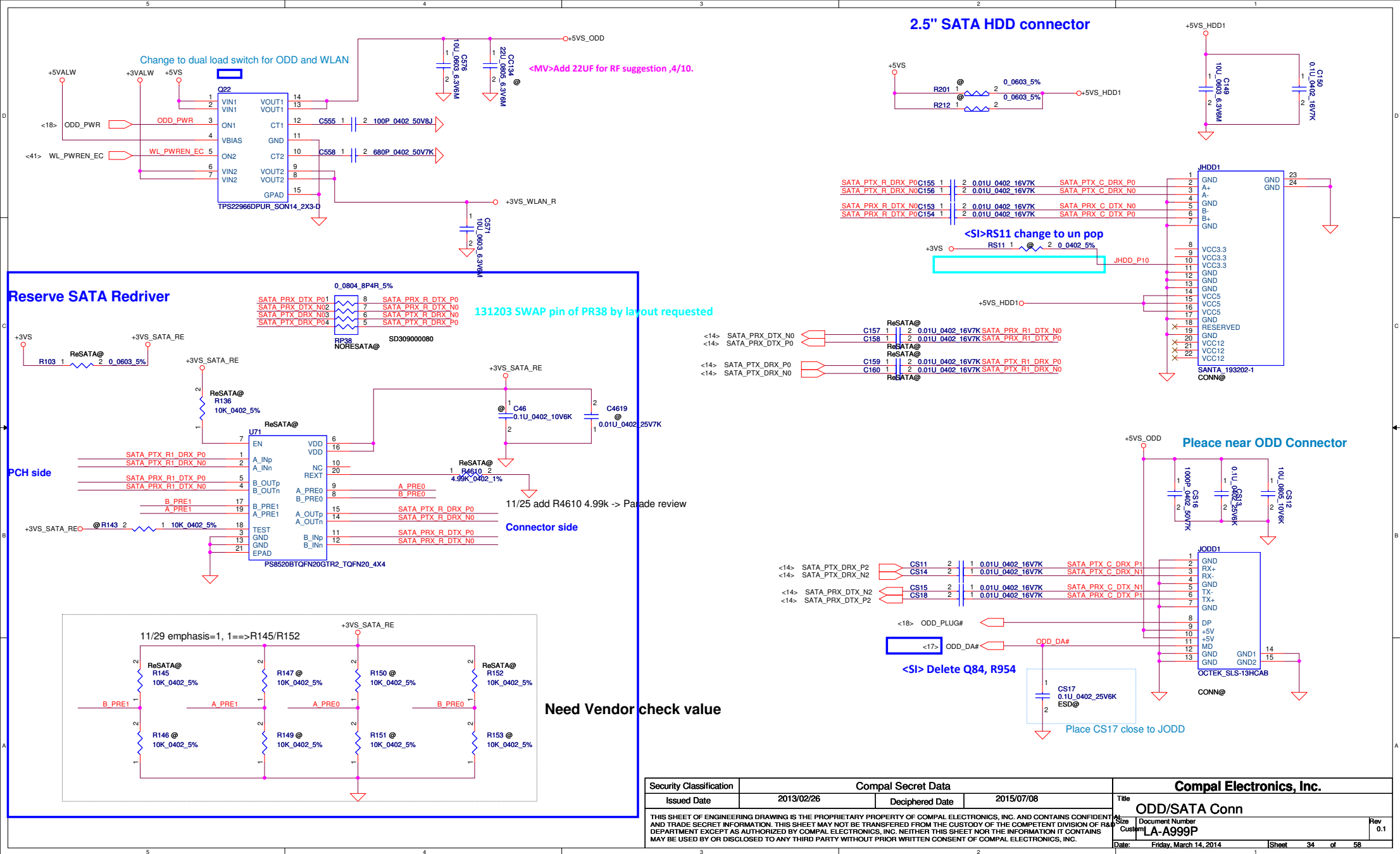
USER Straps	
User [3:0]	
1000-1100	Customer defined

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N15V-GM MISC	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev 1.0
				Date: Friday, March 14, 2014	Sheet 29 of 58	LA-A999P





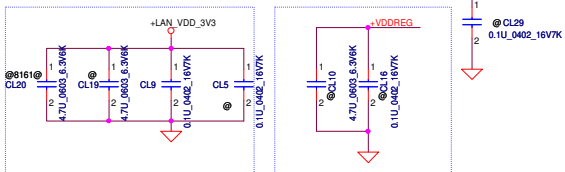
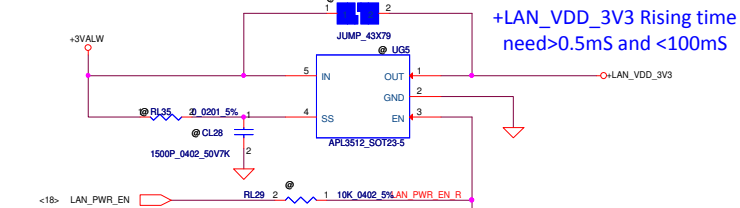
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	WLAN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-A999P	Rev 0.1
Date:	Friday, March 14, 2014	Sheet	33 of 58		



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Customer	0.1
				Date	Friday, March 14, 2014
				Sheet	34 of 58

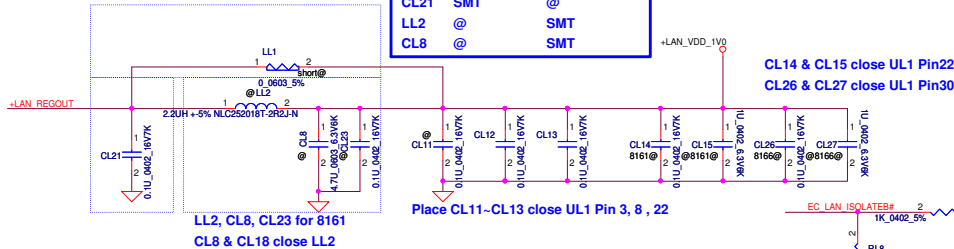
JHW1 need to short

+LAN_VDD_3V3 Rising time need>0.5ms and <100ms



CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11
CL10 & CL16 close to UL1: Pin 23

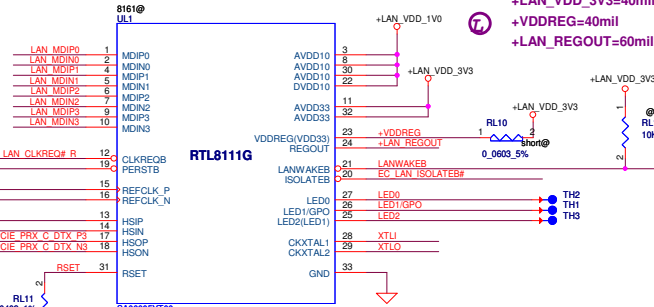
RTL8151G (LDO mode)



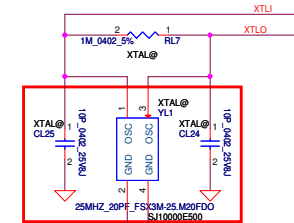
Place CL11-CL13 close UL1 Pin 3, 8, 22

CL14 & CL15 close UL1 Pin22
CL26 & CL27 close UL1 Pin30

8151/8166 Co-Lay

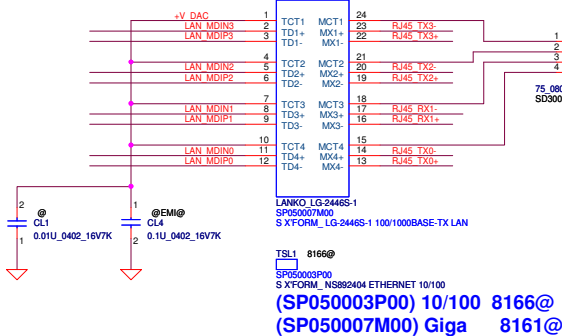


+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



<1118>change to standard part.

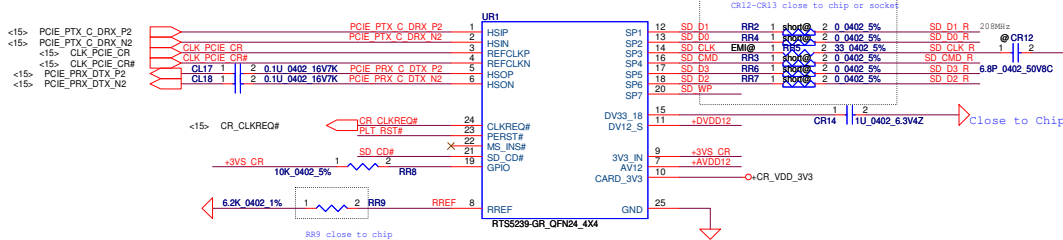
SP050005L00 Footprint



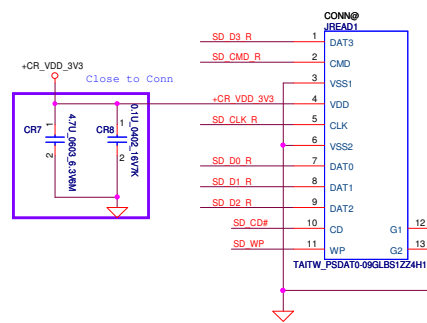
131127 SWAP Pin of DL1.2 & DL1.3 by layout requested

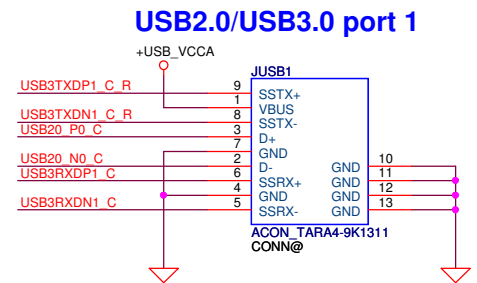
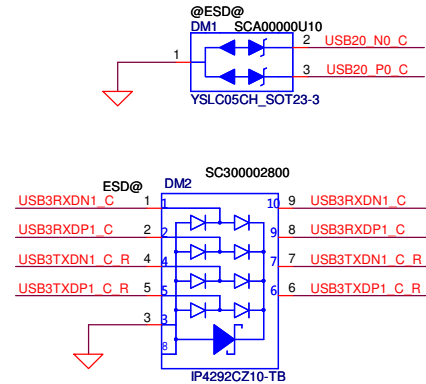
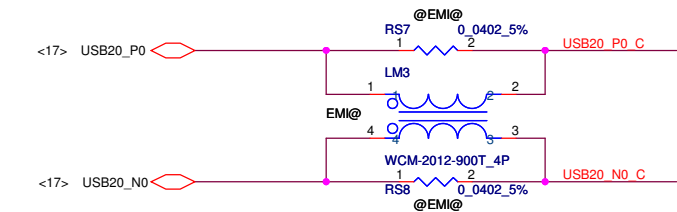
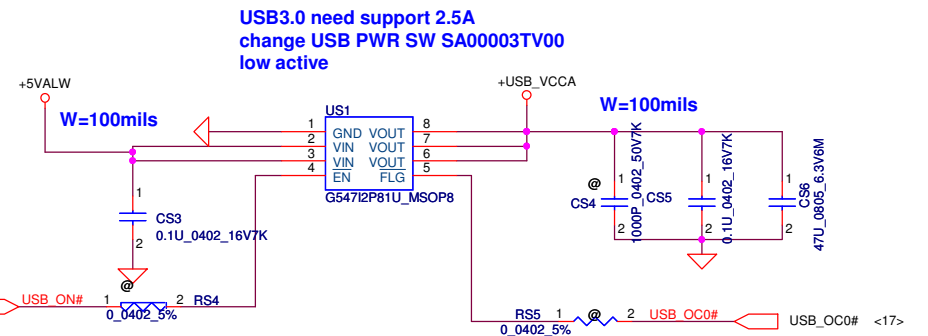
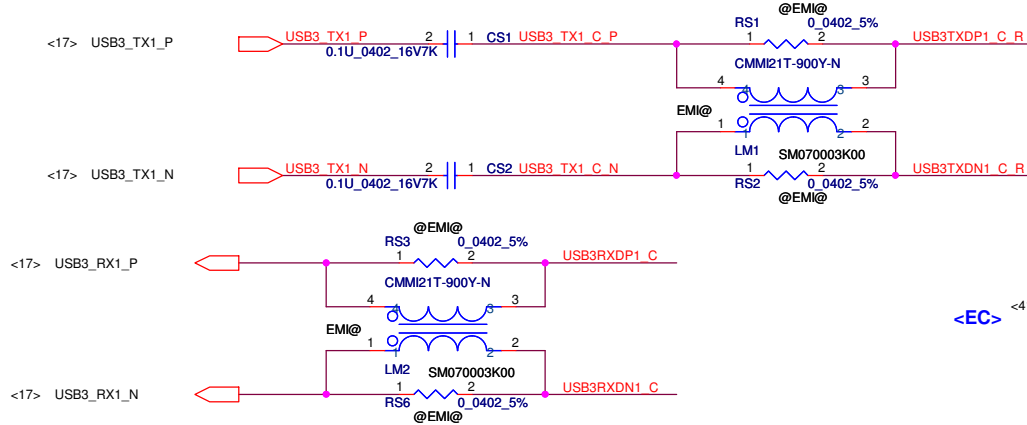
(SA000063500) 10/100 8166@
(SA00005YT00) Giga 8151@

RTS5239

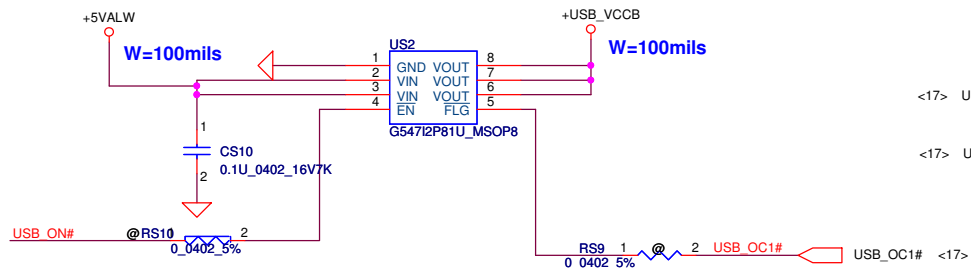


Card Reader Connector

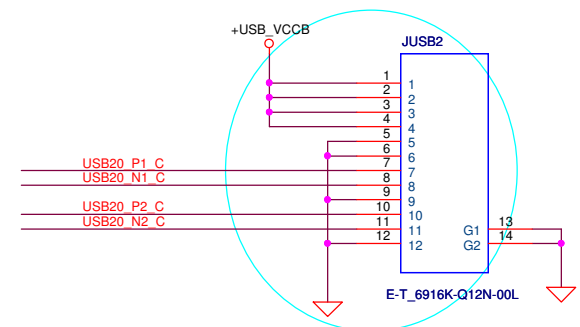




USB2.0 port x 2



131126 reverse the JUSB2, follow haswell 14"



131126 SWAP DM4.2 & DM4.3 by layout requested

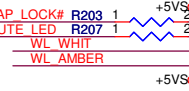
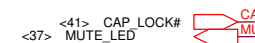
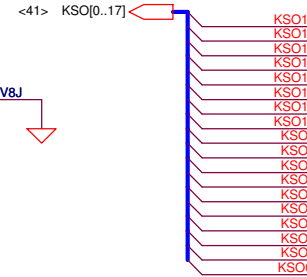
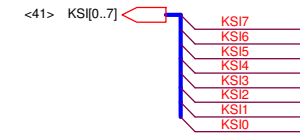
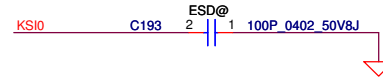
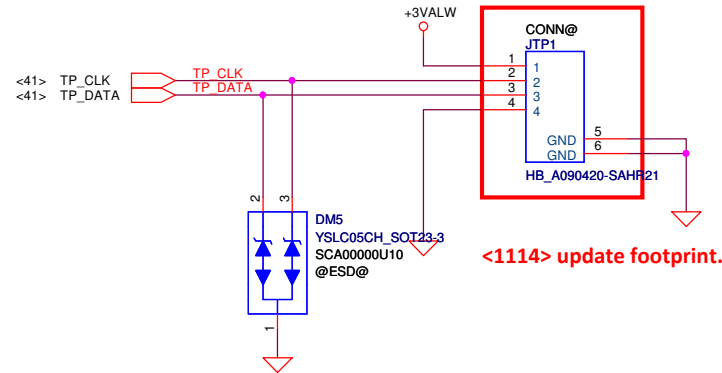


131129 change DM3 & DM4 to pop by ESD requested

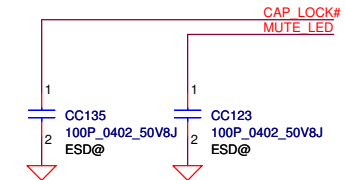
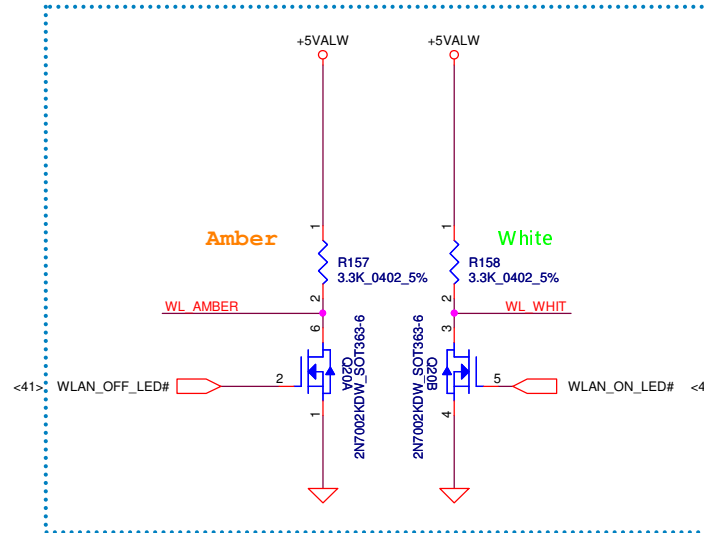
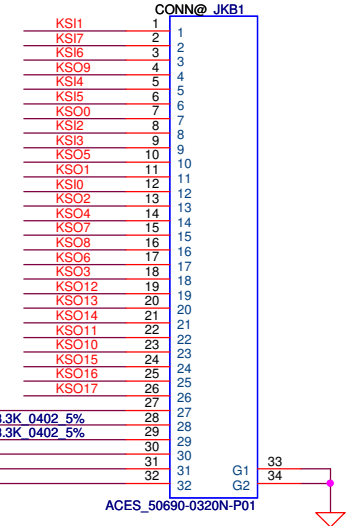
131203 SWAP pin of LM5 by layout requested

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/02/26				Title			
Deciphered Date				2015/07/08				USB 3.0/2.0 conn			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size				Document Number			
				B				LA-A999P			
				Date:				Friday, March 14, 2014			
				Sheet				36 of 58			
								Rev			
								0.1			

Touch pad conn

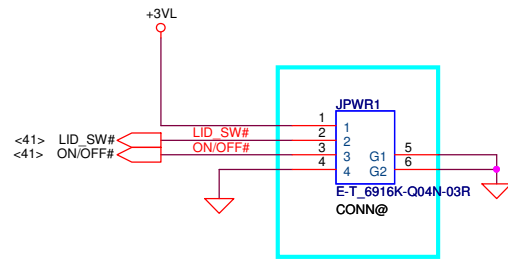


Keyboard conn



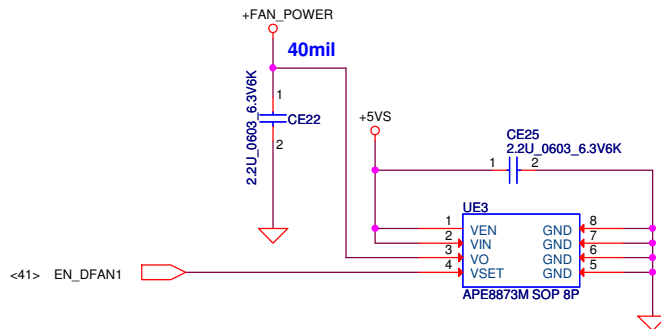
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	KB/TP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number	Rev 0.1
				LA-A999P		
				Date: Friday, March 14, 2014		Sheet 38 of 58

Power Button Connector

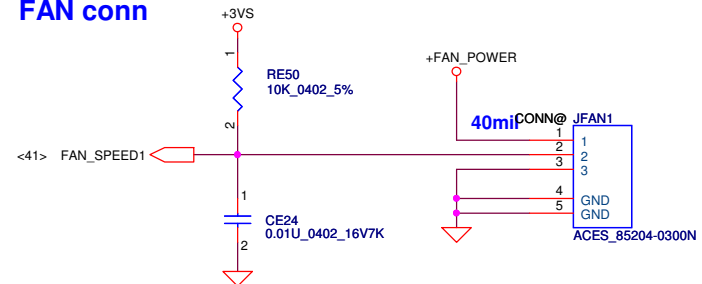


<1205> update footprint.

<SI> Del New Lid SW conn

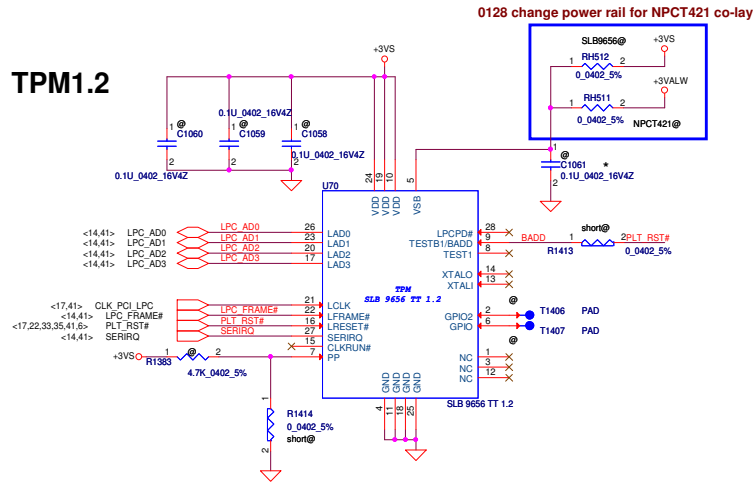


FAN conn

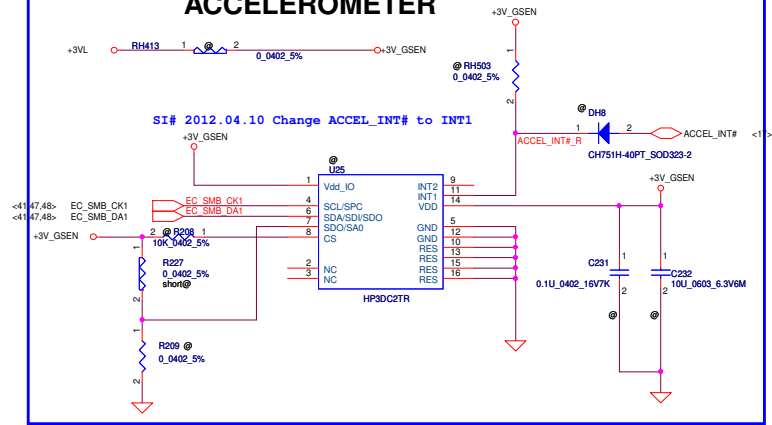


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	PWRBTN/FAN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Rev 0.1
				Document Number	LA-A999P
				Date: Friday, March 14, 2014	Sheet 39 of 58

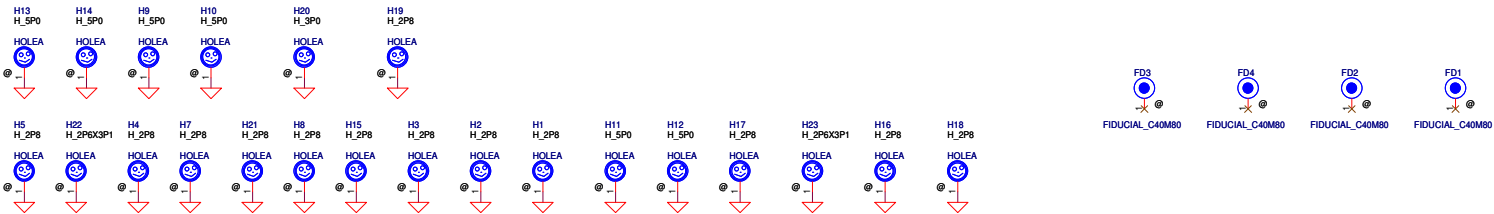
TPM1.2



ACCELEROMETER

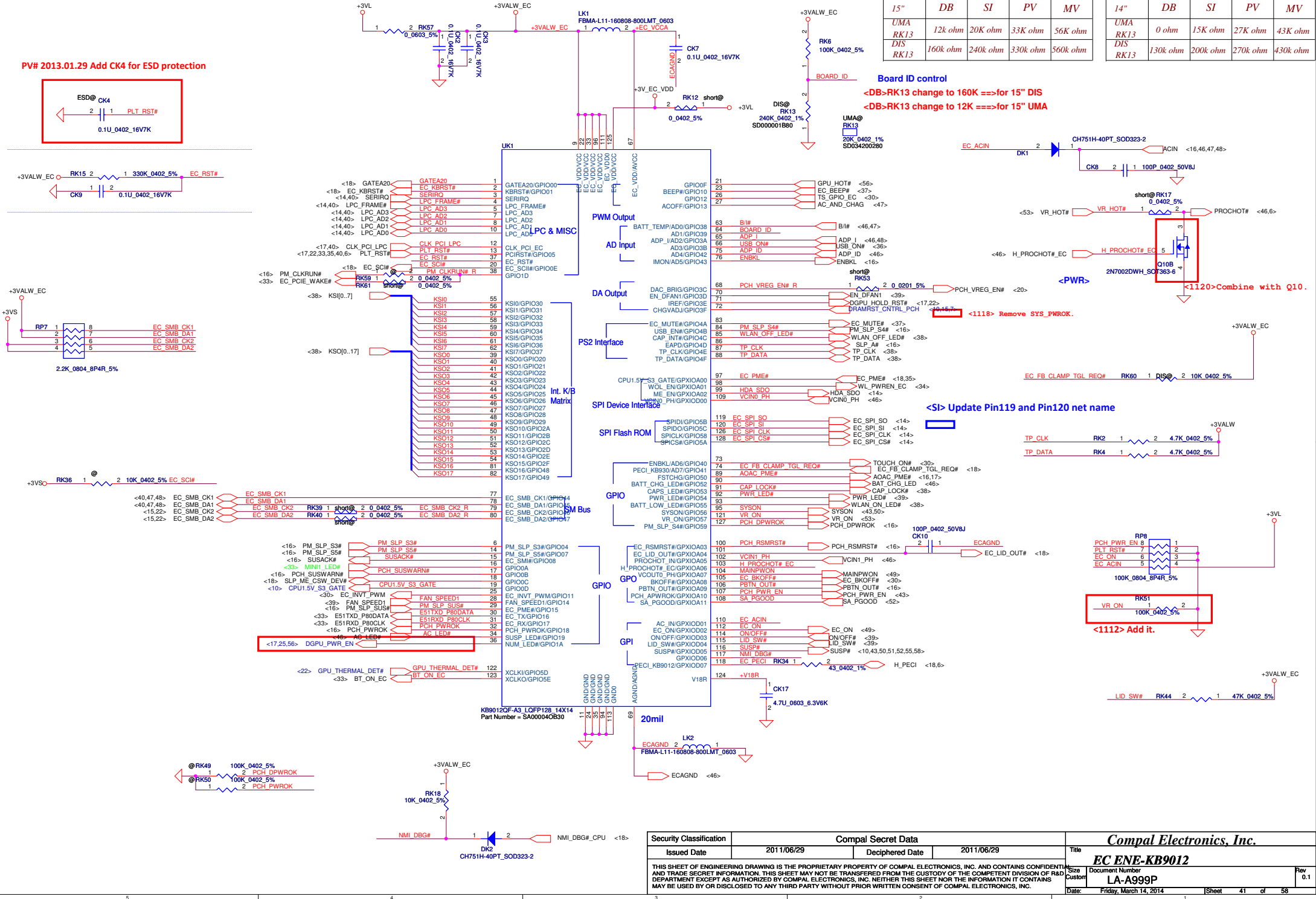
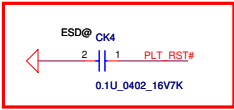


Screw Hole 131127 follow haswell 14"



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	TPM/Screw hole	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					LA-A999P	0.1
				Date:	Friday, March 14, 2014	Sheet 40 of 58

PV# 2013.01.29 Add CK4 for ESD protection



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	EC ENE-KB9012
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-A999P
				Date	Friday, March 14, 2014
				Sheet	41 of 58
				Rev	0.1

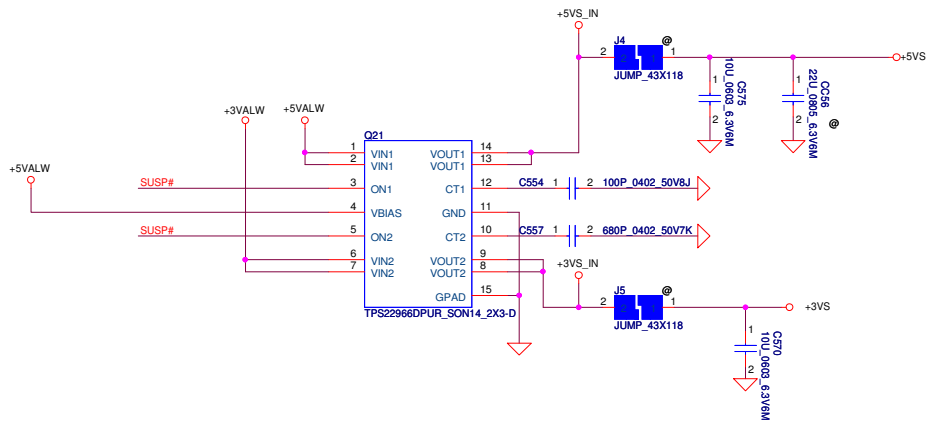
Green CLK no reserved.

BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	25MHz(B)	27MHz	8MHz	Remark
Intel CRV UMA	SLG3NB244VTR	SA000063300	1	1	1	X	X	GCLKUMA@
Intel CRV Dis	SLG3NB304VTR	SA000057I00	1	1	1	1	X	GCLKDIS@

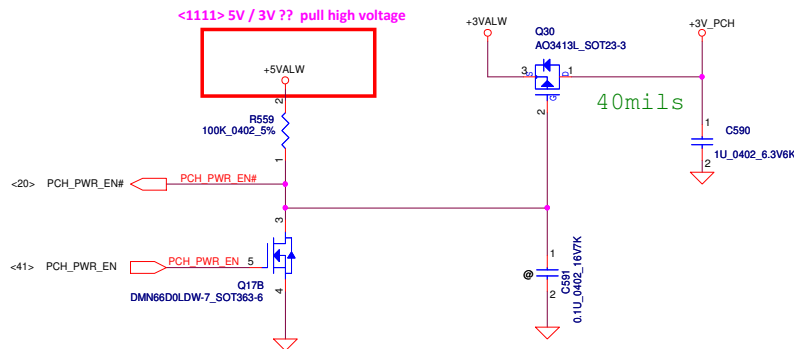
Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

Security Classification		Compal Secret Data		Title <i>Compal Electronics, Inc.</i>	
Issued Date	2013/06/10	Deciphered Date	2014/07/01	Doc No <i>GCLK</i>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number <i>LA-A999P</i>	
				Rev 0.1	
Date: Friday, March 14, 2014		Sheet 31 of 58			



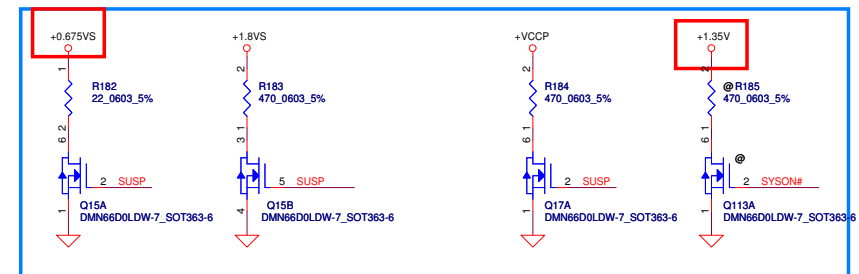
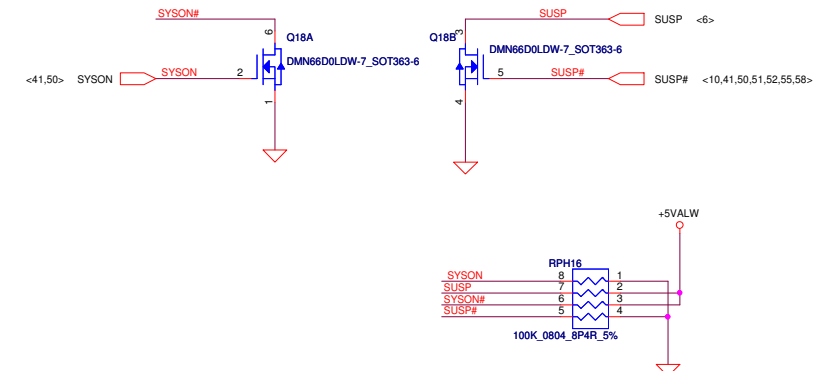
+1.5V to +1.5VS

<1111> Remove +1.5VS DCDC.



AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V

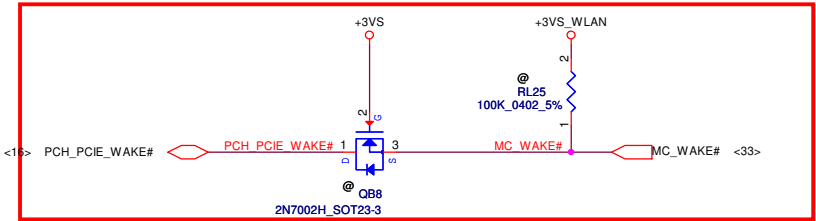
Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V



AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V
Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V

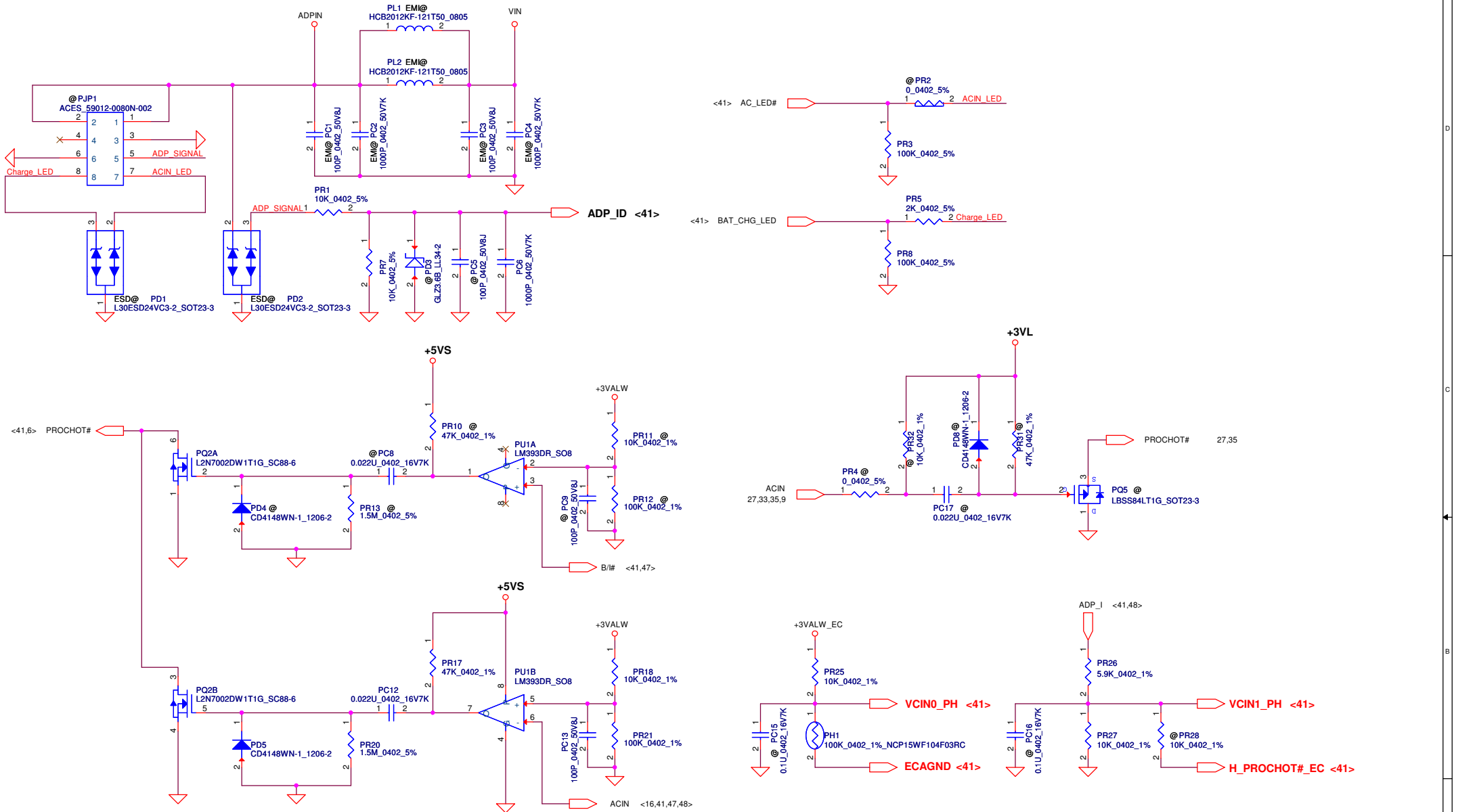
Security Classification				Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title		DC Interface	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev	
				Custom	LA-A999P	0.1	
				Date:	Friday, March 14, 2014	Sheet	43 of 58

NGFF and WLAN

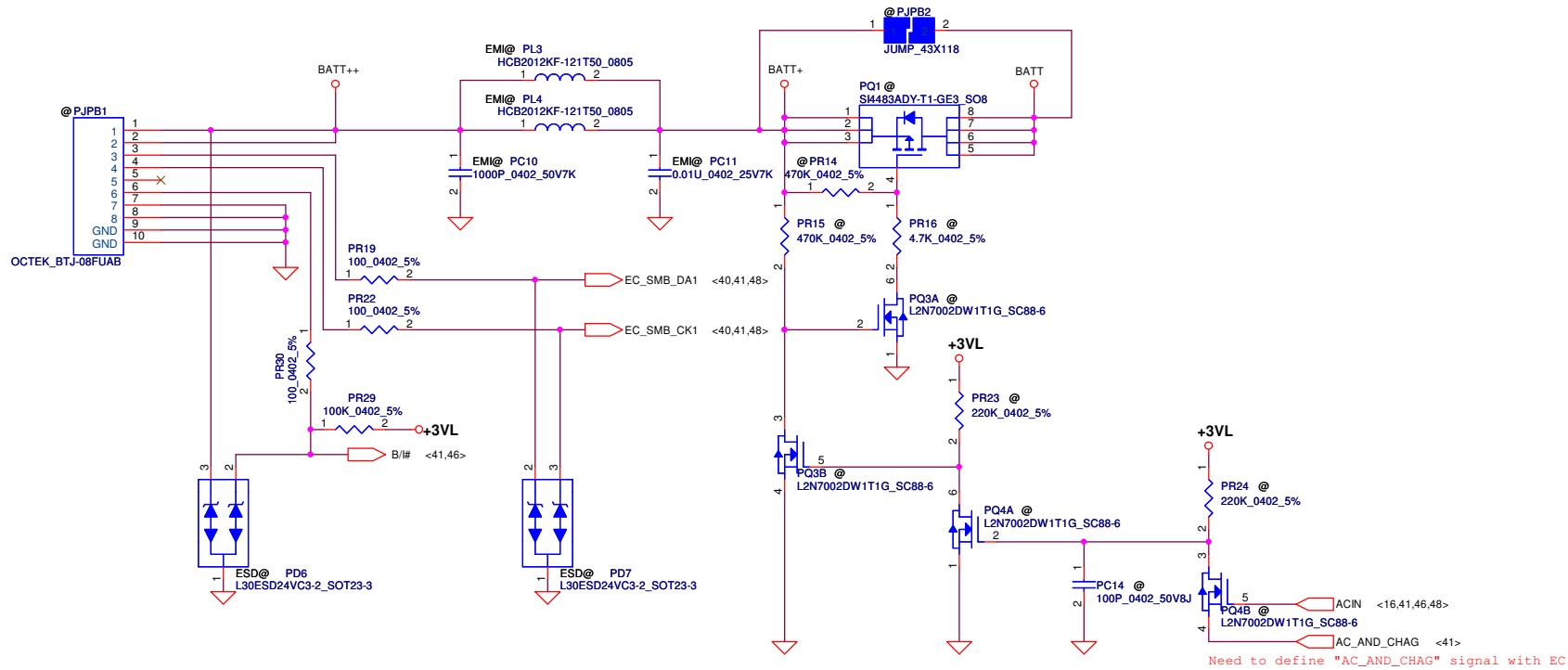


PV# 2013.01.23 Add QB8 abd RL25 to support OBFF
PV# 2013.02.22 Unpop QB4 and RL23 for not support OBFF

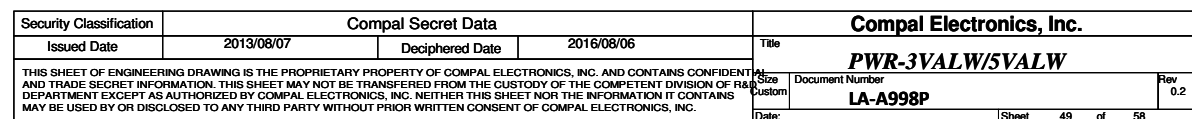
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		WAKE and RST-1		Size Document Number	
				Custom LA-A999P	
				Date: Friday, March 14, 2014	
				Sheet 44 of 58	
				Rev 0.1	

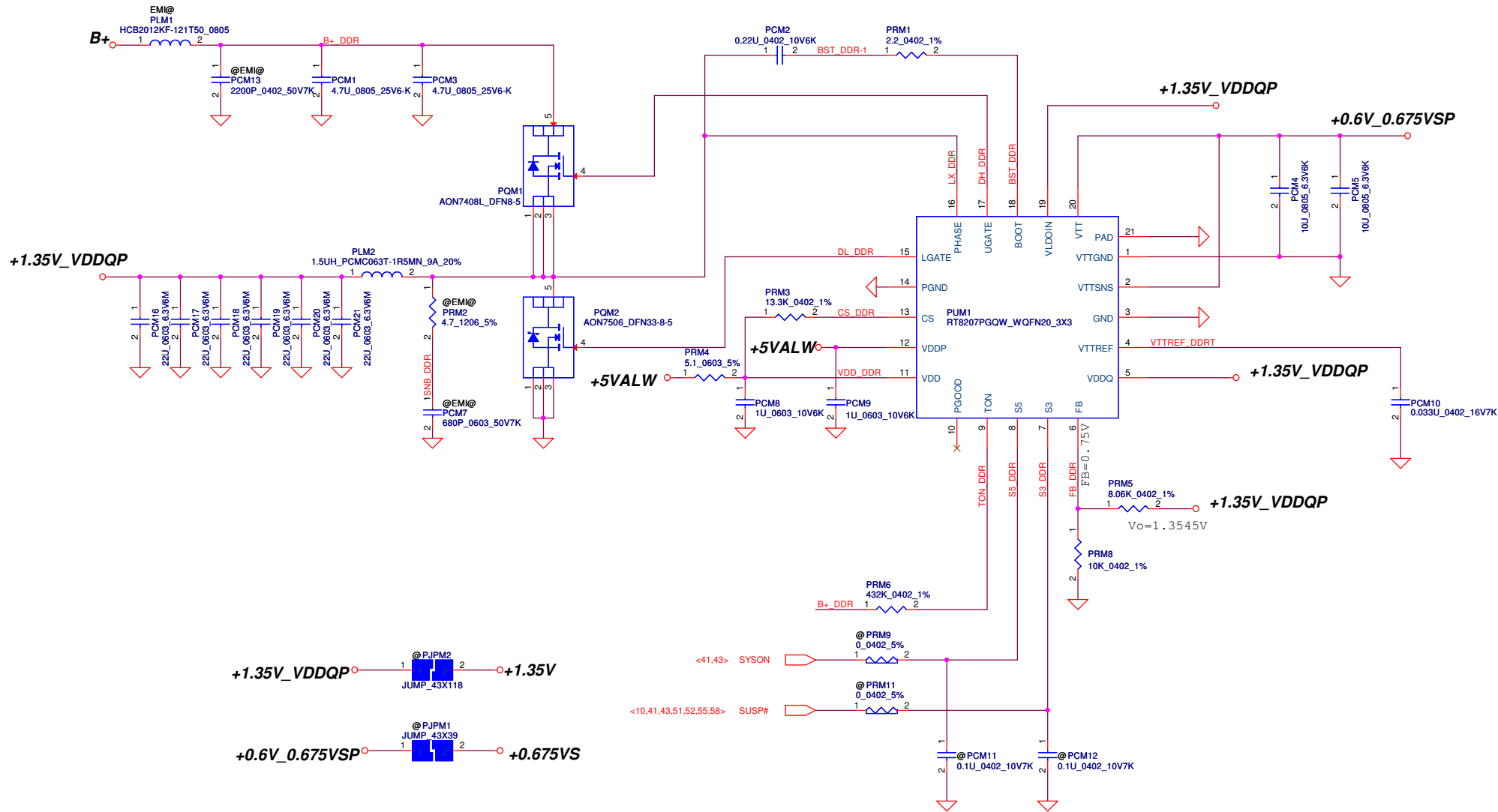


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	PWR-DC Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number LA-A998P
				Rev	0.2
				Date:	Friday, March 14, 2014
				Sheet	46 of 58



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	PWR-BATT Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					LA-A998P
				Date:	Friday, March 14, 2014
				Sheet	47 of 58
				Rev	0.2



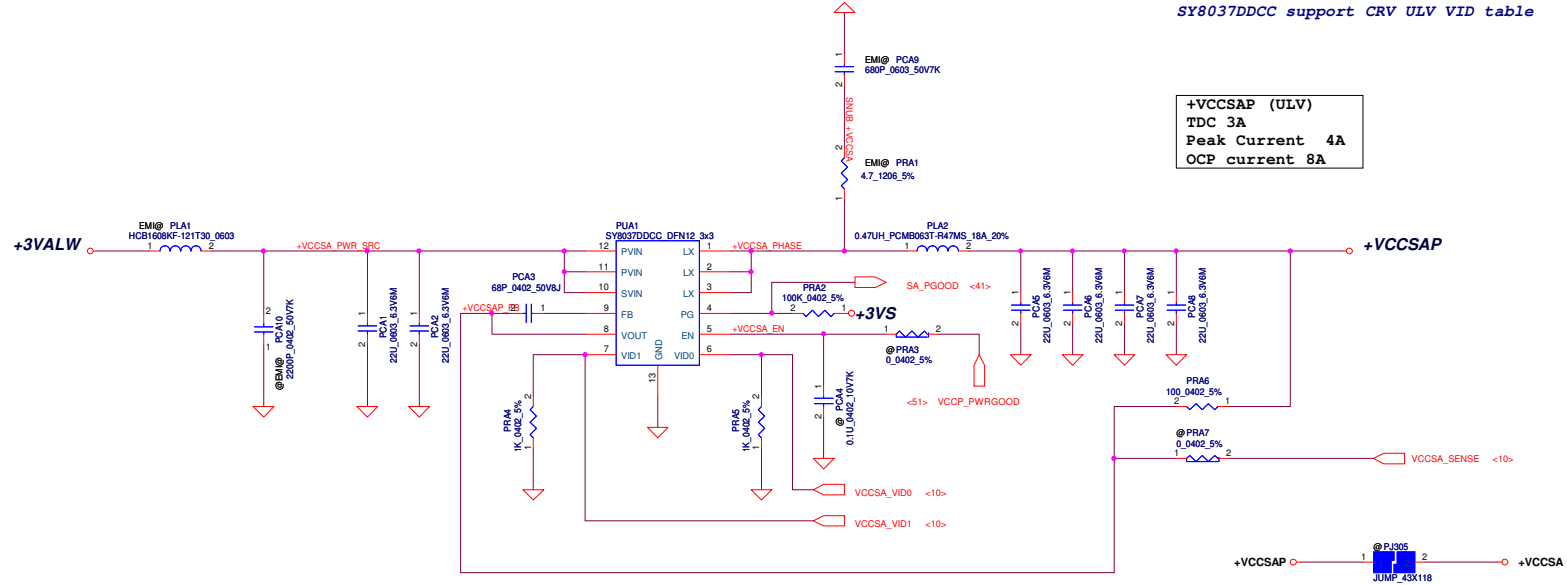


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR-1.35V/0.675VS	
Size	Custom	Document Number	LA-A998P	Rev	0.2
Date:	Friday, March 14, 2014	Sheet	50	of	58

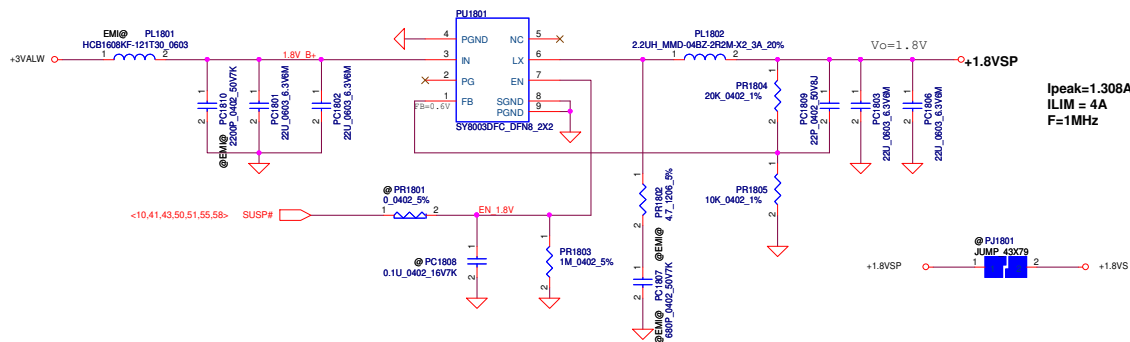
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

SY8037DDCC support CRV ULV VID table

+VCCSAP (ULV)
TDC 3A
Peak Current 4A
OCP current 8A



The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



Ipeak=1.308A
ILIM = 4A
F=1MHz

Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2013/08/07	Deciphered Date
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Title
Size	Document Number	PWR-VCCSAP/1.8VSP
C	LA-A998P	Rev
Date	Friday, March 14, 2014	0.2
Sheet	52	of 58

Design Note
 This circuit is for ULV 1+1 17W.
 CPU: IccMax=33A, TDC=16A(TDP NOM)
 Output Cap. follow Intel PDDG
 330uF/9m*1, 560uF/4.5m*1 22uF_0603*12, 2.2uF_0402*16
 GFX(GT2): IccMax=33A, TDC=21.5A
 Loadline: -3.9 m V/A
 Output Cap. follow Intel PDDG
 560uF/4.5m*1, 22uF_0603*6, 10uF_0603*6, 1uF_0402*11

Close GFX choke

Close GFX L/S MOS

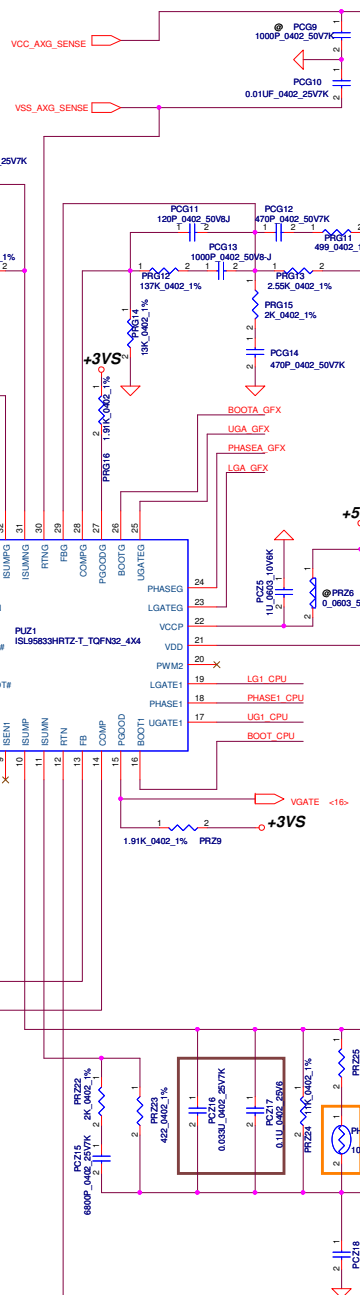
VR_ON
 <=> VR_SVID_CLK
 <=> VR_SVID_ALRT#
 <=> VR_SVID_DAT
 <=> VR_HOT#

For VR_HOT#, already pull high at power side.

PRZ15 and PRG5
 27.4K ohm for 100 degree
 61.9K ohm for 110 degree

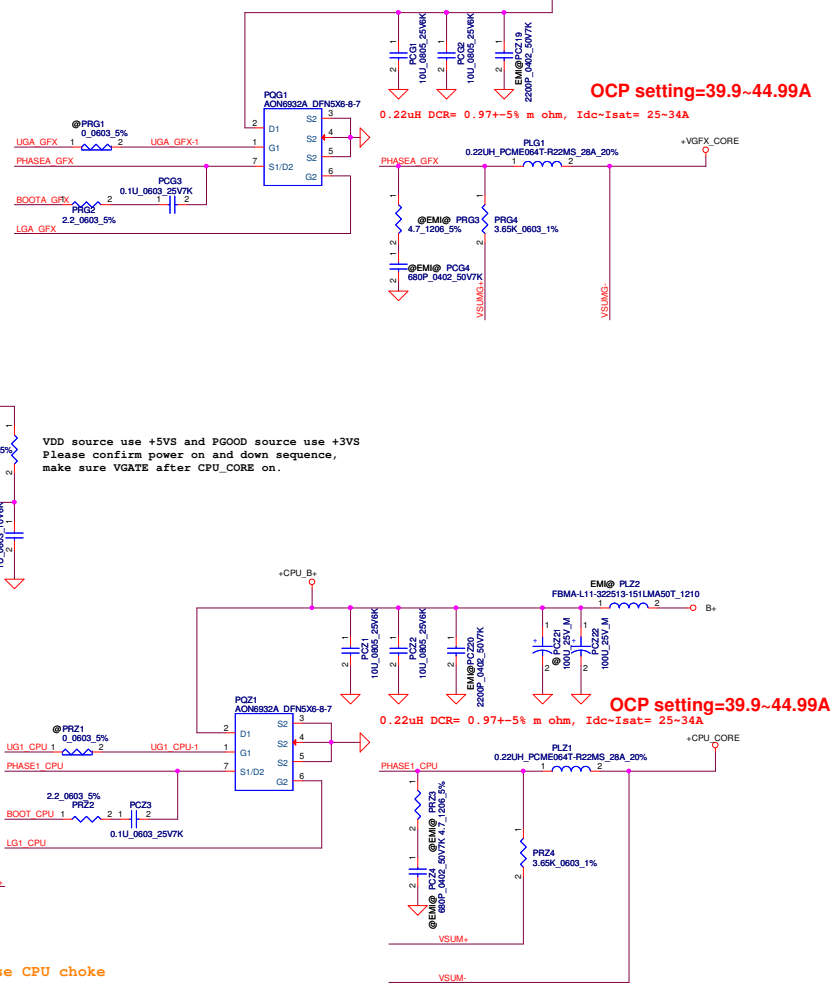
Close CPU L/S MOS

Layout Note
 SVID routing
 1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
 2. SVID spacing requirement is 18mils(0.475mm): VSSENSE
 3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
 4. The SVID bus must be ground reference. It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
 5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.
 6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.



$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$
 If C_n is correctly selected, when the load current has a square change, the output voltage also has a square response.

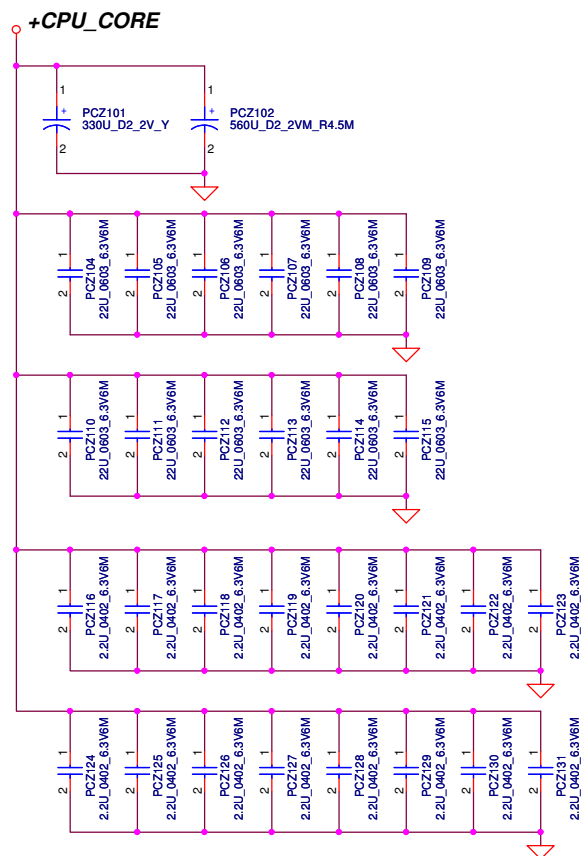
Layout Note
 Reduce Acoustic Noise
 1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
 2. Input ceramic caps must place on symmetry same location on top side and bottom side.



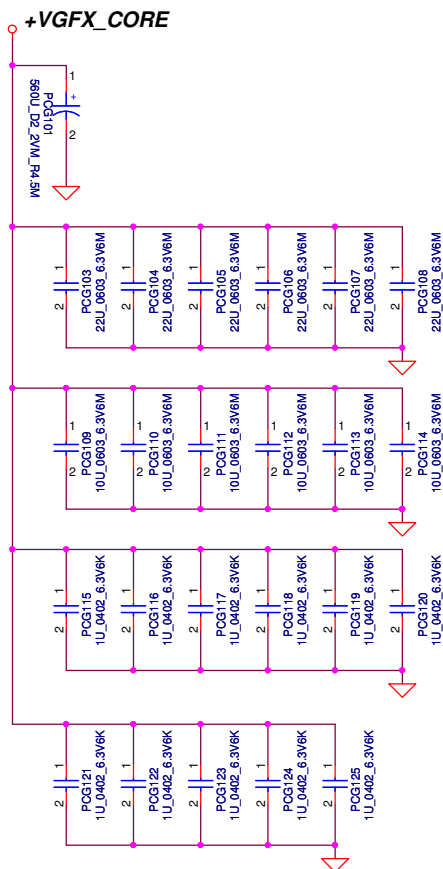
OCP setting=39.9~44.99A

OCP setting=39.9~44.99A

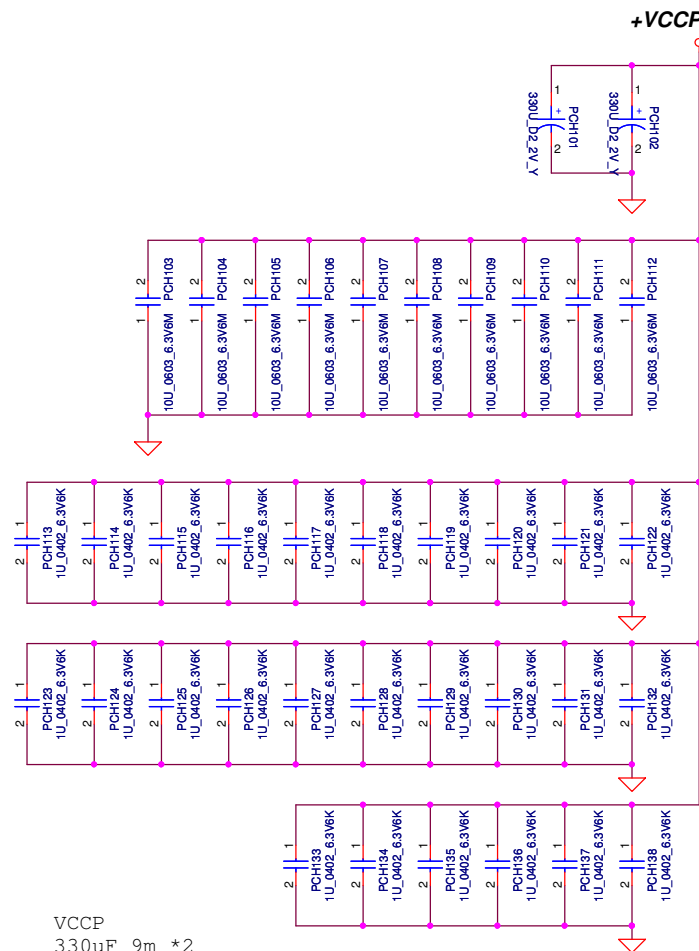
Security Classification	Compal Secret Data		Title	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Rev
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				0.2
Date: Friday, March 14, 2014				Rev
Sheet				53 of 58



```
CPU_CORE
330uF 9m *1
560uF 4.5m *1
22uF 0603 *12
2.2uF 0402 *16
```

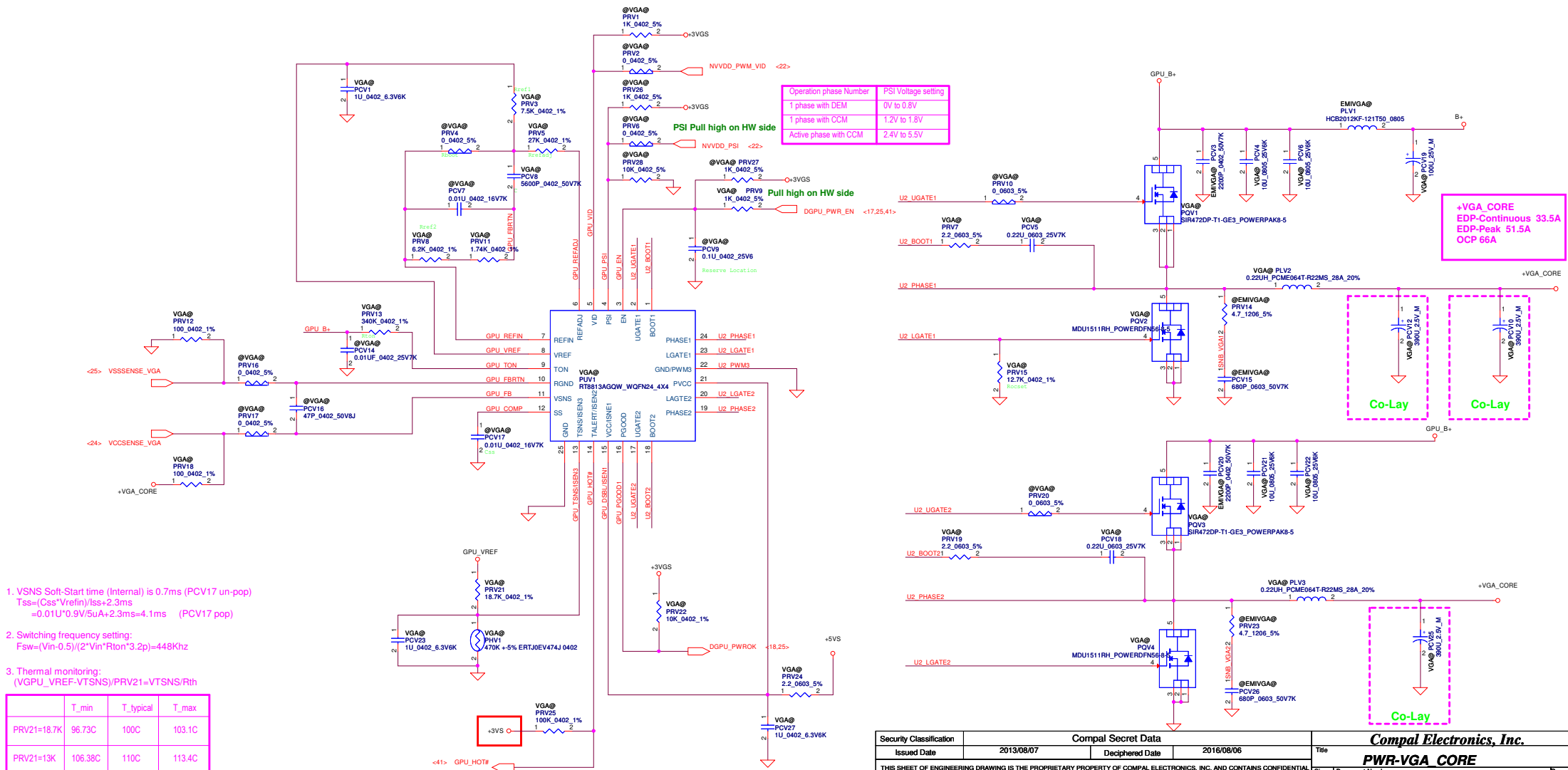


```
GFX_CORE
560uF 4.5m *1
22uF 0603 *6
10uF 0603 *6
1uF 0402 *11
```



VCCP
330uF 9m *2
10uF 0603 *10
1uF 0402 *26

Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR-CPU CORE DECOUPLING	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					LA-A998P
					QFKAA
				Date:	Friday, March 14, 2014
				Sheet	54 of 58
				Rev	0.2



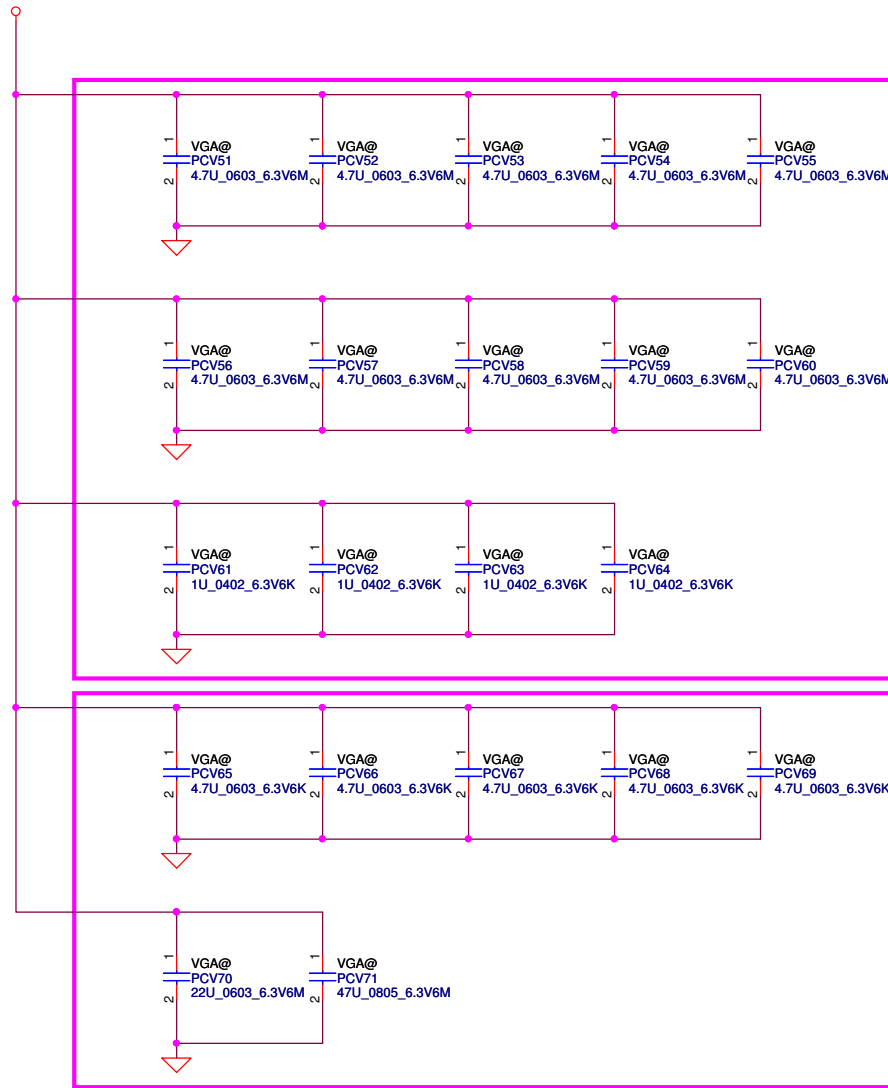
1. VSNS Soft-Start time (Internal) is 0.7ms (PCV17 un-pop)
 $T_{ss} = (C_{ss} \cdot V_{refin}) / I_{ss} + 2.3ms$ (PCV17 pop)
 $= 0.01uF \cdot 0.9V / 5uA + 2.3ms = 4.1ms$ (PCV17 pop)

2. Switching frequency setting:
 $F_{sw} = (V_{in} - 0.5V) / (2 \cdot V_{in} \cdot R_{ton} \cdot 3.2p) = 448KHz$

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PRV21=VTSNS/Rth

	T_min	T_typical	T_max
PRV21=18.7K	96.73C	100C	103.1C
PRV21=13K	106.38C	110C	113.4C

+VGA_CORE



PLACE UNDER GPU

PLACE NEAR GPU

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	PWR-VGA CHIP DECOUPLING
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-A998P
				Date:	Friday, March 14, 2014
				Sheet	57 of 58

